

## TRP10I7HN

# Dual Channel RTD Isolated Temperature Measurement Module Application Notes

Project	Content
Product function	Dual-channel Temperature Acquisition, IIC Signal
Summary of notes	Application Description , Detailed Explanation Of Functions

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## 1. Function Introduction

### 1.1 Summary

TRP10I7HN is a kind of isolated temperature measurement module product for detecting PT100 RTD, which can simultaneously carry out dual-channel temperature detection, and internally adopts 24-bit sigma-delta ADC for signal sampling to ensure high resolution and high accuracy of temperature detection. The module communicates with external devices through the IIC communication interface.

### 1.2 Product Characteristics

- Dual channel PT100 RTD measurement
- Inputs and outputs are isolated from each other (3.75kVAC)
- Temperature measurement error (0.02%±0.1°C)
- High temperature resolution (0.01°C)
- Extremely low temperature drift (15PPM±0.1°C)
- Temperature range (-200°C to +850°C)
- IIC communication interface
- Operating temperature (-40°C to +85°C)
- Small package
- Temperature alarm output

### 1.3 Product Model

Product	Power supply	Input Signal	Output Signal	Measurement range	Package
TRP10I7HN	3.3V	Pt100	IIC Signa	-200°C to +850°C	DIP-16

### 1.4 Applications

- ◆ Industrial thermostats
- ◆ Temperature measuring instruments
- ◆ Temperature monitor
- ◆ High-temperature furnace
- ◆ Steel Heavy Industry
- ◆ Medical equipment
- ◆ Power temperature monitoring
- ◆ Petrochemicals
- ◆ Natural gas pipeline
- ◆ Thermal circulation system

## 2. Hardware Description

### 2.1 Product Appearance

The appearance of the product is shown in Figure 2.1.



Figure 2.1 product appearance drawing

### 2.2 Pin Definition

The TRP10I7HN module has a package size of 25.00\*16.90\*7.10mm and the sensor port is electrically isolated from the communication port. Product definition is shown in Figure 2.2.

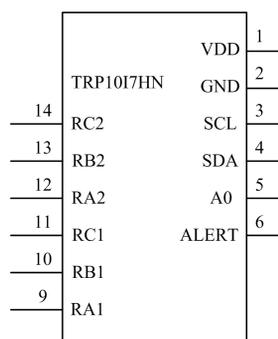


Figure 2.2 Pin arrangement

The pin functions are defined in Table 2.1:

Table 2.1 Pin Function Definition

Pin	Name	I/O	Function
1	VDD	--	Power supply, 3V to 3.6V
2	GND	--	Grounding terminal
3	SCL	I	IIC Communication Clock Pins
4	SDA	I/O	IIC communication data pins
5	A0	I	IIC address select pin, ground (0x48), to VDD or null (0x49)
6	ALERT	O	Alarm signal output pin
9	RA1	--	External RTD PT100 interface, external 1-channel RTD A-terminal
10	RB1	--	External RTD PT100 interface, external 1-channel RTD B-terminal
11	RC1	--	External RTD PT100 interface, external 1-channel RTD C-terminal
12	RA2	--	External RTD PT100 interface, external 2-channel RTD A-terminal
13	RB2	--	External RTD PT100 interface, external 2-channel RTD B-terminal
14	RC2	--	External RTD PT100 interface, external 2-channel RTD C-terminal

2.3 Typical Application Circuit

1) Dual Signal Detection Application Circuit:

TRP10I7HN dual-channel RTD acquisition module as long as a 3.3V DC power supply can work, the signal input is directly connected to the PT100 RTD signal, RA1, RB1, RC1 composed of all the way to the signal acquisition circuit, RA2, RB2, RC2 composed of the other way, the signal output and the standard IIC interface can be connected to realize the dual-channel PT100 RTD signal Acquisition.

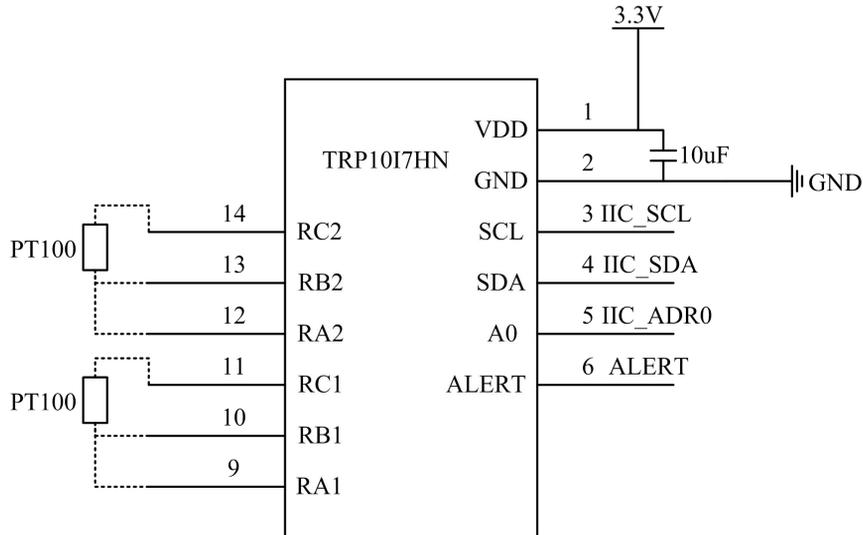


Figure 2.3 Dual Channel Temperature Acquisition Reference Circuit

2) Single signal detection application circuit:

TRP10I7HN dual-channel RTD acquisition module is compatible with single channel signal acquisition. When using single channel signal acquisition, you need to short the signal input of the other channel.

The following figure shows the wiring diagram of the first signal acquisition application circuit.

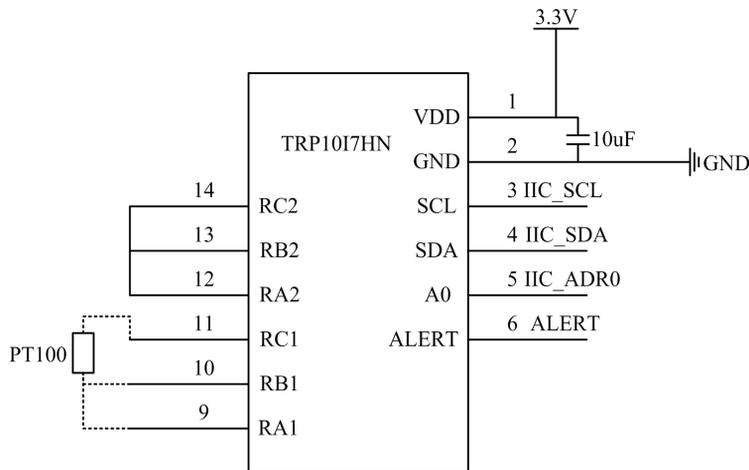


Figure 2.4 Single-channel temperature acquisition reference circuit (1-channel example)

### 3. IIC Bus Description

#### 3.1 IIC Bus Operating Status

- When the bus is idle: both SDA and SCL are held high.
- Start state of data transmission: the state of SDA is from high to low, SCL is kept high, this state is the state of data transmission start.
- End state of data transmission: the state of SDA is from low to high, SCL is kept high, this state is the end state of data transmission.
- Data transmission status: Each byte sent to the SDA line must be 8 bits, the number of bytes that can be sent per transmission is not limited, and each byte must be followed by a response bit. The first bit transmitted is the highest bit (MSB) of the data. If the slave has to complete some other functions (e.g. an internal interrupt service program) before it can receive or send the next complete byte of data, it can keep the clock line SCL low, forcing the host to enter into a wait state, and when the slave is ready to receive a piece of data and releases the clock line SCL, the data transmission continues.
- Acknowledgment Response: the data transmission must be with response and the corresponding response clock pulse is generated by the host. During the response clock pulse, the transmitter releases the SDA line and the receiver must pull the SDA line low so that it remains at a steady low level during the high level of the clock pulse SCL. Normally the addressed receiver must generate a response after receiving each byte in one of the following three cases:
  - ① When the slave cannot respond to the slave address (e.g., it is executing some real-time function and cannot receive or transmit), the slave must hold the data line high, and then the host generates a stop condition to terminate the transmission or a repeat start condition to begin a new transmission.
  - ② If the slave receiver responds to the slave address but cannot receive more data bytes after a period of transmission, the host must again terminate the transmission. This condition is indicated by the slave not generating a response after the first byte. The slave holds the data line high and the host generates a stop or repeat start condition.
  - ③ If there is a host receiver in the transmission, it must notify the slave transmitter of the end of the data by generating a response at the last byte from the slave, and the slave transmitter must release the data line, allowing the host to generate a stop or repeat start condition.
- Clock Synchronization: If the slave wants the host to reduce the transmission speed, it can extend its low level time by actively pulling SCL low, and wait when the host finds that the level of SCL has been pulled low in preparation for the next transmission until the slave completes the operation and releases control of the SCL line. Thus, the host is effectively controlled by the slave's clock synchronization. It can be seen that the low level on the SCL line is determined by the device with the longest low level of the clock, and the high level of the clock is determined by the device with the shortest high level time, which is clock synchronization, which solves the problem of speed synchronization of IIC buses

### 3.2 Data Transmission Process

#### 3.2.1 Host Sending Data Flow

1. The host detects that the bus is "idle" (SDA, SCL line are high), sends a start signal "S", indicating the beginning of a communication;
2. The host then sends a command byte, the byte consists of a 7-bit peripheral device address and a read/write control bit R/W (at this time R/W = 0, write);
3. The corresponding slave receives the command byte, the host back to the answer signal ACK (ACK = 0);
4. The host receives the answer signal from the slave and starts sending the first byte of data;
5. the slave receives the data and returns an answer signal ACK;
6. the host receives the answer signal and then sends the next byte of data;
7. When the host sends the last data byte and receives an ACK from the slave, it ends the communication and releases the bus by sending a stop signal P to the slave. When the slave receives the P signal, it also exits the communication with the host.

The above are the steps for the host to send data. Figure 3.1 shows the schematic diagram of the host sending data.

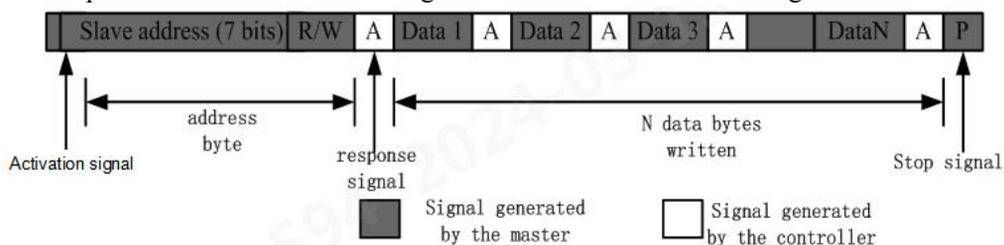


Figure 3.1 Illustration of host sending data

The master communicates with the corresponding slave by sending an address code. Other slaves on the bus, although they also receive the address code, exit communication with the master prematurely because of a mismatch with their own addresses. There is no limit to the amount of data that can be sent in one communication from the master. The host informs the slave of the end of transmission through the P signal, and the slave receives the end signal and exits communication. The host learns about the reception of the slave through the slave's ACK signal after each transmission, and retransmits if there is an answer error.

**3.2.2 Host Receive Data Flow**

1. The host sends a start signal followed by a command byte (where R/W=1: read);
2. the corresponding slave receives the address byte, returns an answer signal and sends data to the host;
3. the host receives the data and returns an answer signal to the slave;
4. The slave receives the answer signal and then sends the next data to the host;
5. When the host has finished receiving data, send a "non-answer signal (ACK=1)" to the slave, and the slave stops sending data after receiving the non-answer signal;
6. The host sends a non-answer signal, and then sends a stop signal to release the bus to end the communication.

The above is the host to receive data steps, Figure 3.2 for the host to receive data schematic.

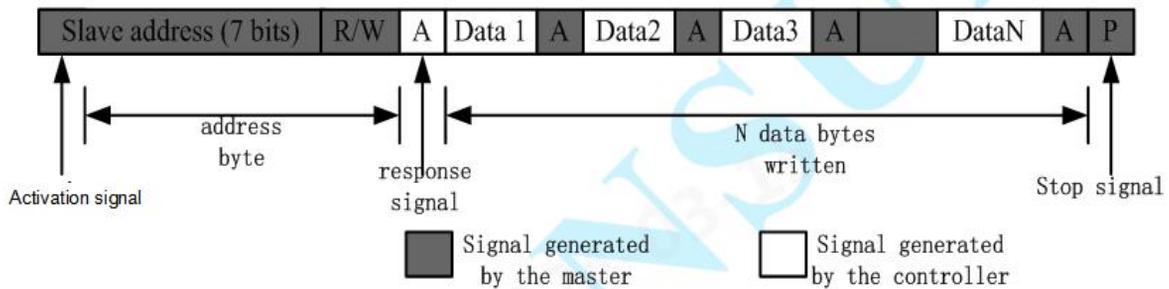


Figure 3.2 Graphical representation of data received by the host

The amount of data received by the host is determined by the host itself. When a "non-answer signal" is sent, the slave terminates the transmission and releases the bus.

(The non-answer signal serves two purposes: ① the previous data was received successfully, and ② the slave is notified not to send any more data).

**3.3 IIC Timing And Registers**

**3.3.1 IIC Timing**

The transmission rate limit of the IIC bus is shown in Figure 3.3.

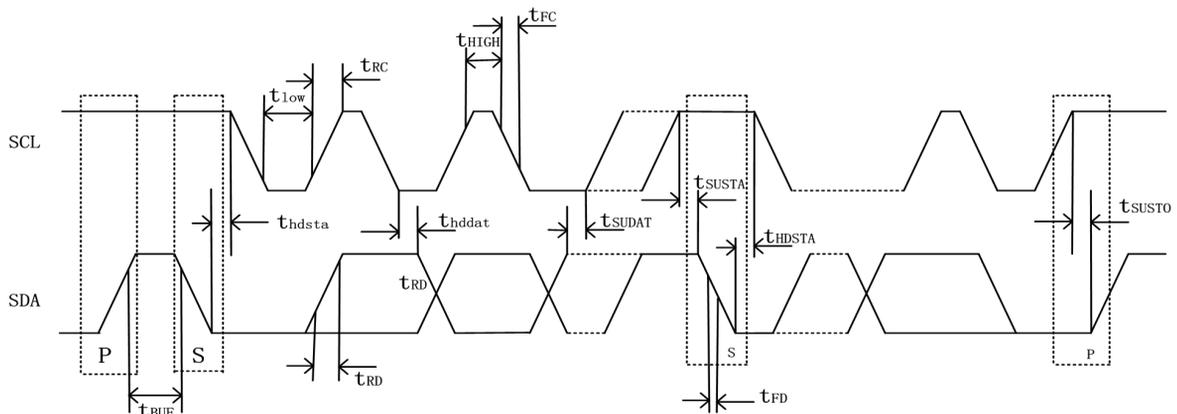


Figure 3.3 IIC Clock and Signaling Time Requirements

Table 3.1 Timing Transmission Time Statistics

Parameters		Value		Unit
		Min.	Max.	
fSCL	SCL operating frequency		100	kHz
tBUF	Idle time for the bus to stop to the startup state	4.7		us
tHDSTA	Hold time after repeated startup until the first clock is generated	4		us
tSUSTA	Repeat start condition establishment time	4.7		us
tSUSTO	Stop condition establishment time	4		us
tHDDAT	Data hold Time	300		ns
tSUDAT	Data setup time	250		ns
tLOW	Clock line low hold time	4.7		us
tHIGH	Clock line high hold time	4		us
tRC, tFC	Clock rise and fall delays		1000, 300	ns
tRD, tFD	Data Rise and fall delay		1000, 300	ns

The IIC bus host sends data timing as shown in Figure 3.4.

<Start -->7-bit slave address, write 0 in last bit (ACK) -->Register subaddress (ACK) -->Write data (ACK) -->Write data (ACK)... -->Stop>

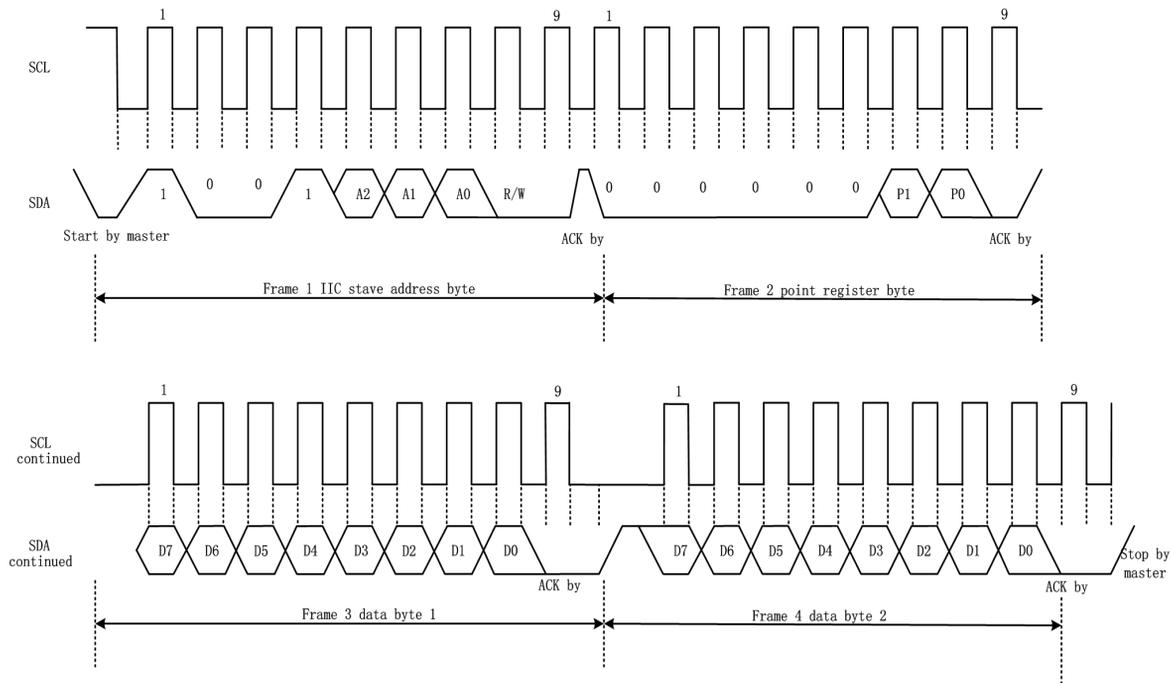


Figure 3.4 Host Sends Data to The TRP10I7HN

When the temperature test module TRP10I7HN communicates outward through the IIC, the test module acts as a slave.

The host receives the TRP10I7HN module data timing diagram shown in Figure 3.5.

<Start-->7-bit slave address, write 0 to the last bit (ACK) -->register subaddress (ACK)

-->Start -->7-bit slave address, last bit write 1 (ACK) -->Read data (ACK) -->Read data (ACK)... -->Stop>

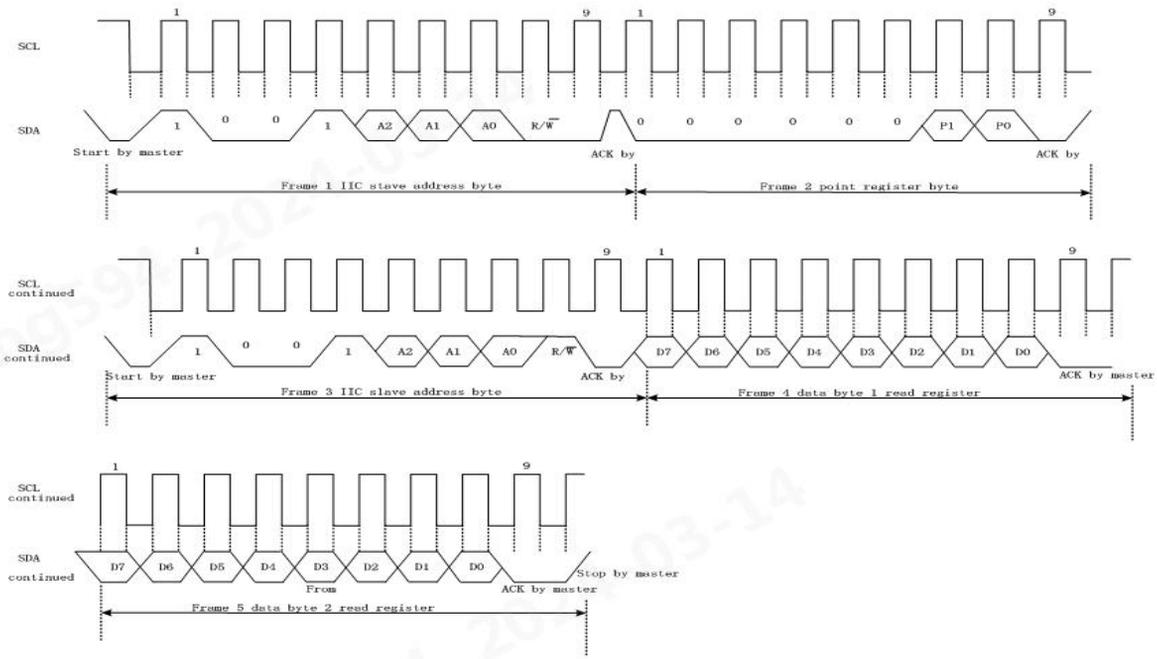


Figure 3.5 Host Receiving TRP10I7HN Data

The address of the IIC of the TRP10I7HN module is different from that in the figure above. Since the TRP10I7HN temperature measurement module has only one address line, the address is set to 100100x, a 7-bit address is used with the higher 6 bits fixed to 100100.

3.3.2 Register Definitions

The internal structure of the registers for the IIC communication protocol of the TRP10I7HN module is shown in Figure 3.6. It is mainly divided into Pointer register, Temperature register, Configuration register, T<sub>LOW</sub> register and T<sub>HIGH</sub> register.

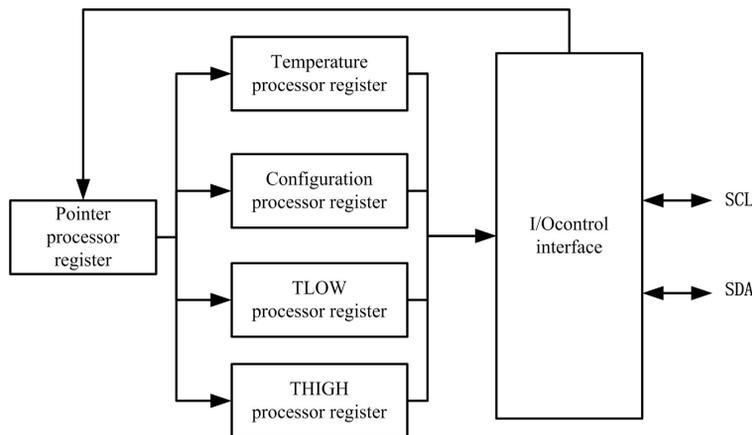


Figure 3.6 Schematic of Register Structure

1. Pointer Register:

Figure 3.6 shows that the primary function of the Pointer register is to indicate the addresses of the other four registers within the TRP10I7HN module. Table 3.2 shows the structural definition of the Pointer register as the last two bits of a byte.

Table 3.2 Pointer Register Internal Structure

P7	P6	P5	P4	P3	P2	P1	P0
0	0	0	0	0	0	Register Bits	

The Pointer register instructions are defined as shown in Table 3.3 and point to each of the four registers in the figure.

Table 3.3 Pointer Register Definition Description

P1	PO	TYPE	processor register
0	0	R only,default	Temperature Register
0	1	R/W	Configuration Register
1	0	R/W	TLOW Register
1	1	R/W	THIGH register

## 2. Temperature Register:

Temperature register contains two 24-bit registers,it contains 6 bytes, as shown below. Table 3.4 shows the correspondence between temperature and register bits. The first 3 bytes of the two registers of Temperature store the temperature test result of channel 1, and the last 3 bytes store the test result of temperature 2. When reading the temperature test result through IIC, 6 bytes are transmitted consecutively, the high byte is transmitted first, and the low byte is transmitted later, and the following writing of the configuration register is also the transmission of the high byte first, and the low byte is transmitted later.

Table 3.4 Temperature Test Value Registers

Channel 1 Temperature Register	Byte	D7	D6	D5	D4	D3	D2	D1	D0
	1	T23	T22	T21	T20	T19	T18	T17	T16
	Byte	D7	D6	D5	D4	D3	D2	D1	D0
	2	T15	T14	T13	T12	T11	T10	T9	T8
	Byte	D7	D6	D5	D4	D3	D2	D1	D0
	3	T7	T6	T5	T4	T3	T2	T1	T0
Channel 2 Temperature Register	Byte	D7	D6	D5	D4	D3	D2	D1	D0
	4	T23	T22	T21	T20	T19	T18	T17	T16
	Byte	D7	D6	D5	D4	D3	D2	D1	D0
	5	T15	T14	T13	T12	T11	T10	T9	T8
	Byte	D7	D6	D5	D4	D3	D2	D1	D0
	6	T7	T6	T5	T4	T3	T2	T1	T0

Table 3.5 Temperature And Register Bit Correspondence

Temperature Value	Digital Output	
	Binary System	Hexadecimal
1023.999878℃	0111 1111 1111 1111 1111 1111	7F FF FFH
0℃	0000 0000 0000 0000 0000 0000	00 00 00H
-0.000122℃	1111 1111 1111 1111 1111 1111	FF FF FFH
-1024℃	1000 0000 0000 0000 0000 0000	80 00 00H

As shown in Table 3.5 for the TRP10I7HN's module, the 24-bit register bits are set to correspond to the temperature, and the 24 bits are assigned as follows: the highest bit is the sign bit, the high 10 bits are used for the integer, and the low 13 bits

are used for the decimal display. The temperature test resolution is 0.000122 °C when using 24 bits. The data conversion is as follows:

Two channels of six bytes of data, the first three bytes of data correspond to channel 1, the last three bytes of data correspond to channel 2, the operation method is the same as that of channel 1, take channel 1 data to analyze as follows:

$$value = Byte1 \ll 16 + Byte2 \ll 8 + Byte3$$

When  $value > 2^{23}$ , the current measured temperature is negative:

$$T = -(2^{24} - value) / 2^{13}$$

When  $value < 2^{23}$ , That is, the current measured temperature is a positive temperature value:

$$T = value / 2^{13}$$

### 3. Configuration Registers

This is the TRP10I7HN operating mode configuration register, which is mainly used to configure the operating mode of the temperature measurement module, as well as the sampling rate. The specific format definition is shown in Table 3.6. Configuration contains two bytes, the first byte configures channel 1, and the second byte configures channel 2.

Table 3.6 Configuration Register Format Definitions

BYTE	D7	D6	D5	D4	D3	D2	D1	D0
1	EN	ALERT	R0	F1	F0	POL	TM	SD
BYTE	D7	D6	D5	D4	D3	D2	D1	D0
2	EN	ALERT	R0	F1	F0	POL	TM	SD

SD: Standby mode reserved bit, now standby mode is not supported, so SD=0.

TM: Alarm signal status control. When TM=0, the alarm signal output is in comparison mode, and when TM=1, the alarm signal output is in interrupt mode.

POL: Alarm pin output signal status control.

Depending on the different values of TM and POL, the product is categorized into four states:

- TM=0, POL=0: Comparison mode, ALERT outputs 1. When the test temperature is greater than THIGH, ALERT becomes 0 until the test temperature is less than TLOW, then ALERT becomes 1.
- TM=0, POL=1: Comparison mode, ALERT outputs 0. When the test temperature is greater than THIGH, ALERT becomes 1 until the test temperature is less than TLOW, then ALERT becomes 0.
- TM=1, POL=0: interrupt mode, ALERT outputs 1, when the test temperature is greater than THIGH, ALERT outputs 0. When the Temperature register is read by an external device, the state of the ALERT output is cleared and changes to the initial state of 1. Until the next time when the temperature test value exceeds the limit, the state of the ALERT changes again.
- TM=1, POL=1: interrupt mode, ALERT output 0, when the test temperature is greater than THIGH, ALERT output is 1. When the Temperature register is read by the external device, the ALERT output state is cleared and changed to the initial state of 0. Until the next time the temperature test value exceeds the limit, the state of ALERT changes again. Details are shown in Figure 3.7.

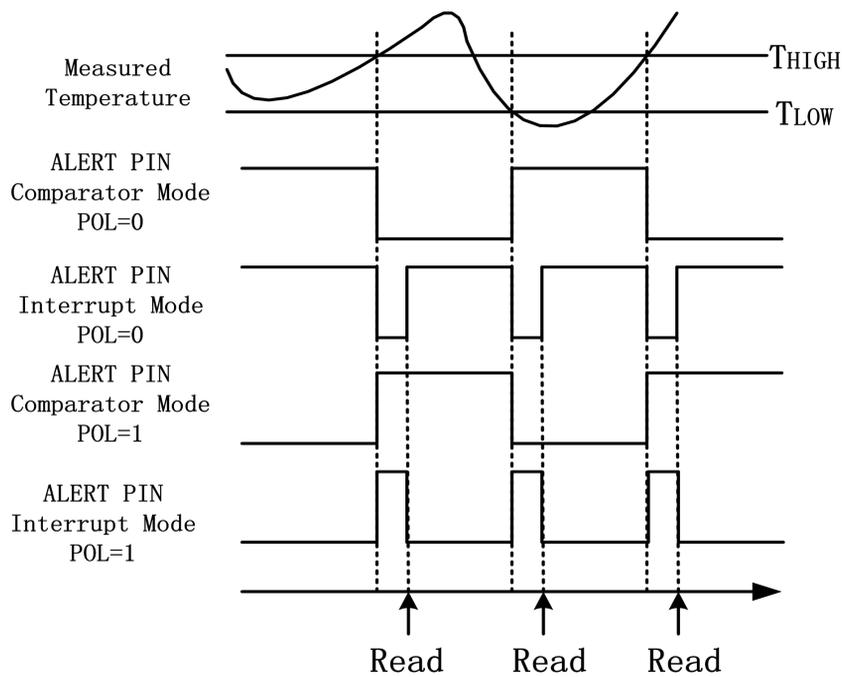


Figure 3.7 Illustration of ALERT Signal Output State Setting

F1, F0: When in the over-temperature or low temperature (beyond the test range) state, trigger the ALERT output signal temperature value test number, specific as shown in Table 3.7, for example, when F1 = 1, F0 = 0, continuous testing of the temperature value of the temperature value of four temperature values are in the case of greater than THIGH, in order to trigger the ALERT output of the corresponding state.

Table 3.7 Number Of Temperature Values Tested To Trigger The ALERT Signal

F1	F0	Number of consecutive faults
0	0	1
0	1	2
1	0	4
1	1	6

R1, R0: control the sampling rate of TRP10I7HN temperature test module, the default is 1s/time;

ALERT: In the comparison mode, read the status of the ALERT bit to determine whether the temperature test value is normal or not.

At the beginning of entering the comparison state, the output state of ALERT is opposite to the POL bit. When POL=1, ALERT=0, until the test temperature value is greater than or equal to TH, ALERT=1, and when the test temperature value is less than TL, ALERT=0. There are two ways to judge the alarm, one is to directly detect the output signal of the ALERT pin, and the other is to judge the temperature test status by reading the ALERT bit in the internal register Configuration of the TRP10I7HN through the IIC.

EN: The configuration is valid when EN=0 and invalid when EN=1. Set the EN of channel 1 as EN1 and the EN of channel 2 as EN2, as shown in Table 3.9.

Table 3.9 Configuration Parameter Selection For Modules

EN1	EN2	Configuration Parameter Selection	Remarks
0	0	Selection of configuration parameters for channel 1	That is, the module works according to byte 1 of the Configurature register
1	1		
0	1		
1	0	Selection of configuration parameters for channel 2	Work according to byte 2 of the Configurature register

For the Configurature register, when not configured by the user, the default is as shown in Table 3.10

Table 3.10 Configuration Default Parameters

BYTE	D7	D6	D5	D4	D3	D2	D1	D0
1	EN	ALERT	R0	F1	F0	POL	TM	SD
	0	* (read-only)	0	1	1	1	0	0(Fixed)
BYTE	D7	D6	D5	D4	D3	D2	D1	D0
2	EN	ALERT	R0	F1	F0	POL	TM	SD
	1	* (read-only)	0	1	1	1	0	0(Fixed)

## 4. THIGH And TLOW Registers

These two registers are to set the upper and lower limits of the test temperature value, both of them are 6 Bytes. the first 3 Bytes are the upper and lower limits of channel 1, and the last 3 Bytes are the upper and lower limits of channel 2, and the registers are stored in the format shown in Table 3.11 and Table 3.12. Each time the temperature test value is compared with THIGH and TLOW, and then ALERT outputs the corresponding signal. External devices can make alarm processing according to this signal. In the initial state, THIGH defaults to 7F FF FFH; TLOW defaults to FF FF FFH.

Table 3.11 THIGH Temperature Register Definitions

Channel 1 THIGN Register	Byte	D7	D6	D5	D4	D3	D2	D1	D0
	1	T23	T22	T21	T20	T19	T18	T17	T16
	Byte	D7	D6	D5	D4	D3	D2	D1	D0
	2	T15	T14	T13	T12	T11	T10	T9	T8
	Byte	D7	D6	D5	D4	D3	D2	D1	D0
3	T7	T6	T5	T4	T3	T2	T1	T0	
Channel 2 THIGN Register	Byte	D7	D6	D5	D4	D3	D2	D1	D0
	4	T23	T22	T21	T20	T19	T18	T17	T16
	Byte	D7	D6	D5	D4	D3	D2	D1	D0
	5	T15	T14	T13	T12	T11	T10	T9	T8
	Byte	D7	D6	D5	D4	D3	D2	D1	D0
	6	T7	T6	T5	T4	T3	T2	T1	T0

Table 3.12 TLOW Temperature Register Definitions

Channel 1 TLOW Register	Byte	D7	D6	D5	D4	D3	D2	D1	D0
	1	T23	T22	T21	T20	T19	T18	T17	T16
	Byte	D7	D6	D5	D4	D3	D2	D1	D0
	2	T15	T14	T13	T12	T11	T10	T9	T8
	Byte	D7	D6	D5	D4	D3	D2	D1	D0
Channel 2 TLOW Register	3	T7	T6	T5	T4	T3	T2	T1	T0
	Byte	D7	D6	D5	D4	D3	D2	D1	D0
	4	T23	T22	T21	T20	T19	T18	T17	T16
	Byte	D7	D6	D5	D4	D3	D2	D1	D0
	5	T15	T14	T13	T12	T11	T10	T9	T8
	Byte	D7	D6	D5	D4	D3	D2	D1	D0
6	T7	T6	T5	T4	T3	T2	T1	T0	

#### 4. Notes Of Product Using

- ◆ Does not support hot plug
- ◆ For a more in-depth understanding of the electrical parameters of the TRP10I7HN product, please refer to the TRP10I7HN Technical Manual.

#### 5. Disclaimer

Dual-channel RTD Isolated Temperature Measurement Module TRP10I7HN copyright all belongs to MORNSUN Guangzhou Science & Technology Co., Ltd., and its property rights are absolutely protected by national laws. Without the authorization of this company, other companies, units, agents and individuals are not allowed to illegally use and copy it, otherwise it will be severely punished by national laws. If you need our products and related information, please contact us in time. MORNSUN Guangzhou Science & Technology Co., Ltd. reserves the right to revise the user manual at any time without notice.