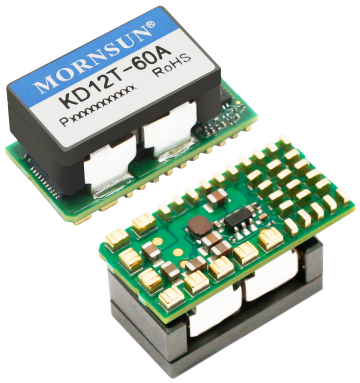
Non-isolated & regulated 60A single/30A dual output POL Digital Regulators



Patent Protection RoHS

- Differential remote sense
- Tracking and output voltage sequencing
- Input UV and output OV/UV protection
- Output OCP
- Over temperature protection
- Black-box fault recording

FEATURES

- Small Package 25.4 x 12.7 x 12.96 mm
- Flexible solution for single or dual output configuration
- Wide input voltage range: 7.5 to 14.4VDC
- Wide output voltage range: 0.6 to 4.5VDC
- High output voltage deviation: ±10mV
- Low output ripple and noise: 7mVp-p
- High maximum output current, 60A per output for single output or 30A for dual output
- High efficiency, typ. 92%
- Current sharing up to 2 modules, 120A
- Fast load transient response: 30mV
- Wide operating temperature range -40℃ to 85℃
- Configuration and monitoring via PMBus
- Fixed switching frequency with capability of an external synchronization

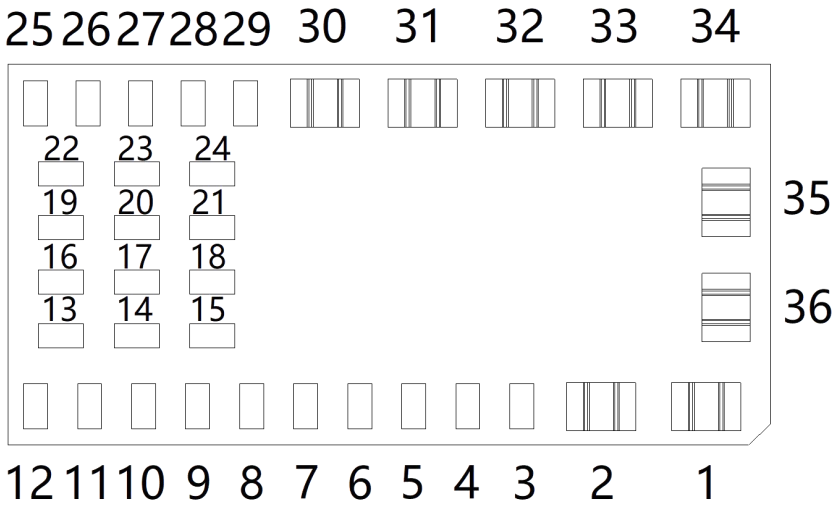
The KD12T-60A Digital modules are non-isolated DC-DC converters that can deliver up to 60A single/30A dual of output current. The modules operate over a 7.5 to 14.4VDC input range and provide an adjustable, precisely regulated output voltage from 0.6 to 4.5VDC. Output voltage is programmable via an external resistor divider or PMBus command. Features include the PMBus digital protocol, remote CNTL, Power Good, over-current, under-voltage, over-voltage and over-temperature protection. It includes a real-time compensation loop for optimizing the dynamic response to match the load. It is widely used in communications, computer network industries, and power distributed architecture, workstations, servers, LANs/WANs, providing high current with fast transient response for high-speed chips of FPGA, DSP and ASIC.

Selection Guide

Certification	Part No.	Input Voltage (VDC)	Output		Output voltage accuracy (mV) Max.	Ripple & Noise (mVp-p) Typ.
		Nominal (Range)	Voltage (VDC) Nominal (Range)	Current (A) Max.		
--	KD12T-60A	12 (7.5-14.4)	0.6-4.5	60	±10	7

CONTENT

Pin-out Descriptions

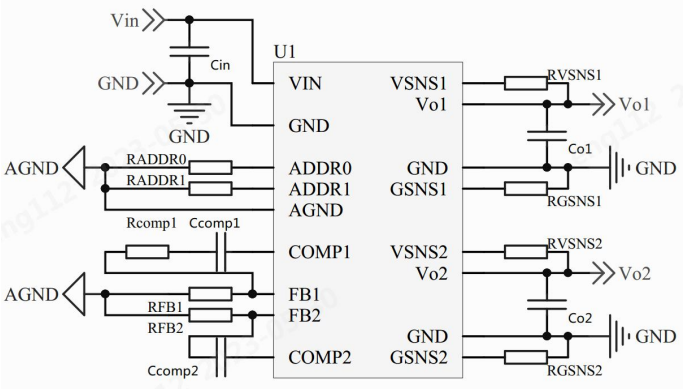


Pin layout, bottom view.

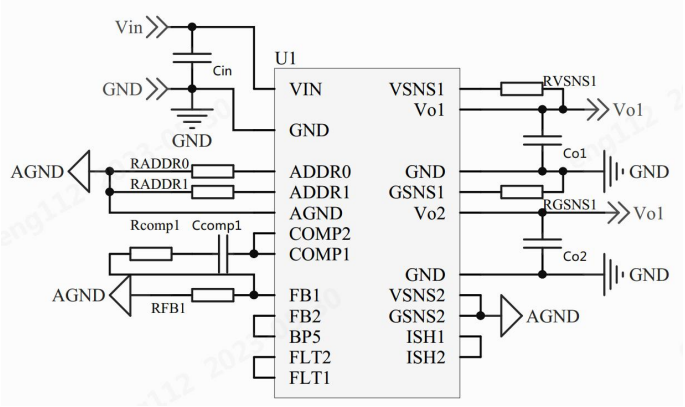
Pin	Designation	Type	Function
1, 36	VIN	Power	Input voltage.
2	GND	Power	Power ground.
3	PG2	O	Open drain power good indicator for channel 2 output voltage. This pin is pulled to ground internally in slave channel.
4	PG1	O	Open drain power good indicator for channel 1 output voltage. This pin is pulled to ground internally in slave channel.
5	CNTL2	I	Logic level input which starts or stops channel 2. An internal 6-μA current source pulls V_{CNTL2} up to V_{BP5} when the pin is floating.
6	CNTL1	I	Logic level input which starts or stops channel 1. An internal 6-μA current source pulls V_{CNTL1} up to V_{BP5} when the pin is floating.
7	SYNC	I/O	This is the synchronization pin for use with the external clock. The frequency of external SYNC signal must be 4 times of desired switching frequency during 1-, 2-, or 4- phases, and must be 3 times the desired switching frequency during 3-phase configuration.
8	NC	/	NC.
9	ADDR1	I	High order address pin for PMBus device. Connect a resistor to GND (see PMBus Address).
10	PMBCLK	I	PMBus clock pin.
11	PMBDATA	I/O	PMBus data pin
12	SMBALERT	O	PMBus alert pin.
13	AGND	/	AGND.
14	COMP1	O	Output of the error amplifier 1 and connection node for loop feedback components.
15	FLT1	I/O	Fault signal of channel 1.
16	NC	/	NC.
17	PHSET	I/O	Phase set for multi-phase mode.
18	ISH1	I	Current sharing signal of channel 1 for multi-phase mode.
19	BP5	O	Output bypass for the internal regulator.
20	ADDR0	I	Low order address pin for PMBus device. Connect a resistor to GND (see PMBus Address).
21	ISH2	I	Current sharing signal of channel 2 for multi-phase mode.

22	FB2	I	Inverting input to the error amplifier 2. In normal operation, the voltage on this pin is equal to the internal reference voltage. Connect the FB2 pin to the BP5 pin to set the channel as slave channel.
23	FLT2	I/O	Fault signal of channel 2.
24	COMP2	O	Output of the error amplifier 2 and connection node for loop feedback components.
25	VSENS2	I	Positive pin of voltage sense signal for channel 2.
26	GSENS2	I	Negative pin of Voltage Sense Signal for channel 2.
27	FB1	I	Inverting input to the error amplifier 1. In normal operation, the voltage on this pin is equal to the internal reference voltage. Connect the FB1 pin to the BP5 pin to set the channel as slave channel.
28	GSENS1	I	Negative pin of Voltage Sense Signal for channel 1.
29	VSENS1	I	Positive pin of voltage sense signal for channel 1.
30, 31	VO2	Power	Output voltage 2.
32	GND	Power	Power ground of channel 2.
33, 34	VO1	Power	Output voltage 1.
35	GND	Power	Power ground of channel 1.

Typical Application Circuit



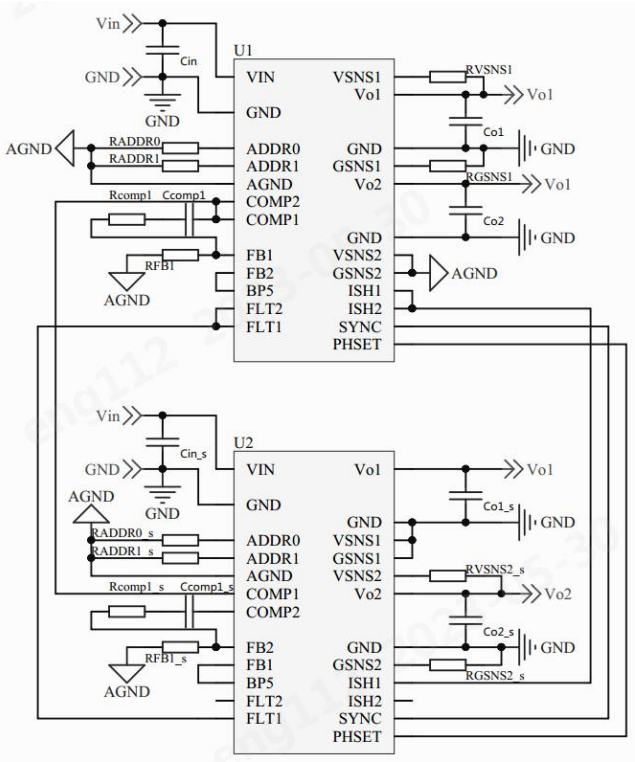
Dual output



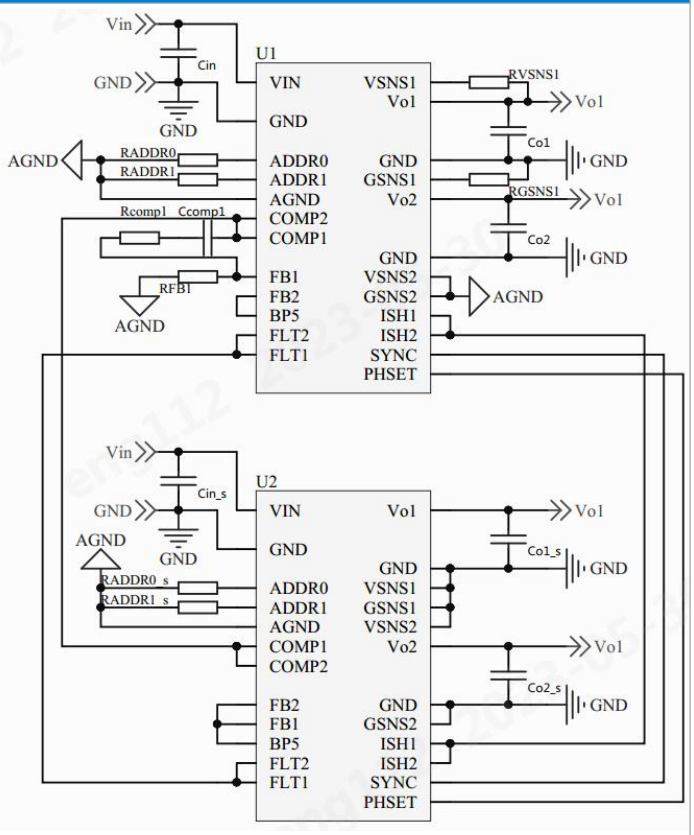
2-PHASE/SINGLE OUTPUT

PIN NAME	DUAL OUTPUT	2-PHASE / SINGLE OUTPUT
SYNC	Floating or connect to external clock	Floating or connect to external clock
PHSET	Floating	Floating
FB1	Inverting input to the error amplifier of CH1	Inverting input to the error amplifier of CH1
FB2	Inverting input to the error amplifier of CH2	Connect to BP5
COMP1	Output of the error amplifier of CH1	Output of the error amplifier of CH1, connect to COMP bus
COMP2	Output of the error amplifier of CH2	Connect to COMP bus
ISH1	Floating	Connect to ISH bus
ISH2	Floating	Connect to ISH bus
FLT1	Fault inductor of CH1	Connect to FLT bus
FLT2	Fault inductor of CH2	Connect to FLT bus
PG1	Power good indicator for CH1 output voltage, connect to BP5 via a pull-up resistor	Power good indicator for 2-phase output voltage,connect to BP5 via a pull-up resistor
PG2	Power good indicator for CH2 output voltage, connect to BP5 via a pull-up resistor	Floating or connect to GND
VSENS1	Positive pin of Voltage Sense Signal for CH1	Positive pin of Voltage Sense Signal for 2-phase output
GSENS1	Negative pin of Voltage Sense Signal for CH1	Negative pin of Voltage Sense Signal for 2-phase output
VSENS2	Positive pin of Voltage Sense Signal for CH2	Connect to GND is recommended. Connect to the output voltage is also allowed.
GSENS2	Negative pin of Voltage Sense Signal for CH2	Connect to GND
CNTL1	Logic level input which starts or stops CH1	Logic level input which starts or stops both channels.
CNTL2	Logic level input which starts or stops CH2	Floating

Typical Application Circuit



3-PHASE



4-PHASE

Typical Application Circuit

DEVICE	PIN NAME	3-PHASE	4-PHASE
Master /U1	SYNC	Connect to SYNC bus	Connect to SYNC bus
	PHSET	Connect to PHSET bus	Connect to PHSET bus
	FB1	Inverting input to the error amplifier for CH1 of Master	Inverting input to the error amplifier for CH1 of Master
	FB2	Connect to BP5 of Master	Connect to BP5 of Master
	COMP1	Output of the error amplifier for CH1 of Master connect to COMP bus	Output of the error amplifier for CH1 of Master, connect to COMP bus
	COMP2	Connect to COMP bus	Connect to COMP bus
	ISH1	Connect to ISH bus	Connect to ISH bus
	ISH2	Connect to ISH bus	Connect to ISH bus
	FLT1	Connect to FLT bus	Connect to FLT bus
	FLT2	Connect to FLT bus	Connect to FLT bus
	PG1	Power good indicator for 3-phase output voltage,connect to BP5 via a pull-up resistor	Power good indicator for 4-phase output voltage, connect to BP5 via a pull-up resistor
	PG2	Floating or connect to GND	Floating or connect to GND
	VSENS1	Positive pin of Voltage Sense Signal for 3-phase output	Positive pin of Voltage Sense Signal for 4-phase output
	GSENS1	Negative pin of Voltage Sense Signal for 3-phase output	Negative pin of Voltage Sense Signal for 4-phase output
	VSENS2	Connect to GND is recommended. Connect to the output voltage is also allowed.	Connect to GND is recommended. Connect to the output voltage is also allowed.
	GSENS2	Connect to GND	Connect to GND
	CNTL1	Logic level input which starts or stops 3-phase	Logic level input which starts or stops 4-phase
	CNTL2	Floating	Floating

Typical Application Circuit

DEVICE	PIN NAME	3-PHASE	4-PHASE
Slave /U2	SYNC	Connect to SYNC bus	Connect to SYNC bus
	PHSET	Connect to PHSET bus	Connect to PHSET bus
	FB1	Connect to BP5 of Slave	Connect to BP5 of Slave
	FB2	Inverting input to the error amplifier for CH2 of Slave	Connect to BP5 of Slave
	COMP1	Connect to COMP bus	Connect to COMP bus
	COMP2	Output of the error amplifier for CH2 of Slave	Connect to COMP bus
	ISH1	Connect to ISH bus	Connect to ISH bus
	ISH2	Floating	Connect to ISH bus
	FLT1	Connect to FLT bus	Connect to FLT bus
	FLT2	Fault indicator for CH2 of Slave	Connect to FLT bus
	PG1	Floating or connect to GND	Floating or connect to GND
	PG2	Power good indicator for CH2 output voltage of Slave, connect to BP5 via a pull-up resistor	Floating or connect to GND
	VSENS1	Connect to GND is recommended. Connection to the output voltage is also allowed.	Connect to GND is recommended. Connection to the output voltage is also allowed.
	GSENS1	Connect to GND	Connect to GND
	VSENS2	Positive pin of Voltage Sense Signal for CH2 of Slave	Connect to GND is recommended. Connect to the output voltage is also allowed.
	GSENS2	Negative pin of Voltage Sense Signal for CH2 of Slave	Connect to GND
	CNTL1	Connect to CNTL1 of Master	Connect to CNTL1 of Master
	CNTL2	Logic level input which starts or stops CH2 of Slave	Floating

Note :

1.The corresponding input voltage range is 10-14.4V;

2.The recommended peripheral parameters are as follows:

Devices	DUAL OUTPUT	2-PHASE	3-PHASE	4-PHASE
Rcomp1	NC	0Ω/0603		
Ccomp1	NC	470pF/16VDC	1000pF/16VDC	
Ccomp2	NC	470pF/16VDC	470pF/16VDC	/
Rcomp1_s	/	/	NC	/
Ccomp1_s	/	/	NC	/
RVSNS1，RGSNS1 RVSNS2，RGSNS2	10Ω/0603			
RFB1(_s)，RFB2(_s)	Refer to "Output Voltage Regulation" on page 35			
RADDR0(_s), RADDR1(_s)	Refer to the PMBus Address Bits section on page 32			
Cin(_s)	2x470 uF/10 mΩ OS-CON + 8 x 10 uF ceramic capacitor			
Co1(_s)，Co2(_s)	For single-phase or multiphase applications, output per phase：4 x 330 uF/10 mΩ Polymer + 10 x 100 uF ceramic capacitor,			

Absolute Maximum Ratings

		Min.	Max.	UNIT
Voltage	Vin	-0.3	16	V
	BP5、FB、PG、CNTL、COMP、FLT	-0.3	7	V
	GSNS、VSNS、PMBDATA、SMBALERT、PMBCLK、SYNC、ISH、PHSET	-0.3	5.5	V
	ADDR	-0.3	3.6	V
Temperature	Operating temperature (see Thermal Consideration section)	-40	85	℃
	Storage temperature	-55	125	℃
Humidity	Storage Humidity (Non-condensing)	5	95	%RH
Operating altitude		--	2000	m
Reflow Soldering Temperature	IPC/JEDEC J-STD-020D.1.	Peak temperature ≤245℃, duration ≤60s max. over 217℃		
Moisture Sensitivity Level (MSL)	IPC/JEDEC J-STD-020D.1	MSL 3		
Pollution Degree		PD 3		
Vibration		IEC/EN61373 - Category 1, Grade B		

Note:

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Configuration File

This product is designed using a digital control circuit. The control circuit uses a configuration file which determines the functionality and performance of the product. The Electrical Specification table shows parameter values of functionality and performance with the Standard configuration, unless otherwise specified. The Standard configuration is designed to fit most application needs. Changes in Standard configuration might be required to optimize performance in specific application. Note that current sharing operation requires changed configuration.

Common Electrical Specification

Typically, these are parameters related to the digital controller of the products. In the table below, PMBus commands for configurable parameters are written in capital letters.

Operating temperature is -40 to +85 ℃, Vin = 7.5 to 14.4 V, unless otherwise specified under Conditions.

Typical values given at: Operating temperature is +25 ℃, Vin = 12.0 V, max Io, unless otherwise specified under Conditions.

Vo defined by pin strap. Standard configuration.

Characteristics		Conditions	Min.	Typ.	Max.	Unit
FREQUENCY AND SYNCHRONIZATION						
f	Switching frequency (default value)		--	430	--	kHz
	Switching frequency range(1)	Pin-strap (SYNC)	200	--	1500	kHz
	SYNC high-level threshold(2)		2	--	--	V
	SYNC low-level threshold(2)		--	--	0.8	V
	Minimum SYNC pulse width		--	100	--	ns
(1) There are configuration changes to consider when changing the switching frequency. Changing switching frequency might have other impacts, please check with FAE. (2) The external SYNC pin signal must be a square waveform with 50% duty cycle.						
INITIALIZATION TIME AND SOFT-START						
T_{INI}	Initialization time	after BP5 voltage is ready	--	1	--	ms
t_{ss}	Soft-start time(1)	Default settings	--	2.7	--	ms
	Programmable range		0.6	--	9	ms
	Accuracy over range		-15	--	15	%
(1) The soft-start time is the time that the internal reference voltage rises from 0 V to 600 mV.						
PGOOD						
V_{FBPGH}	FB PGOOD high threshold	Default settings	--	642	--	mV
V_{FBPGL}	FB PGOOD low threshold	Default settings	--	558	--	mV
$V_{PG(acc)}$	PGOOD accuracy over range		-4	--	4	%
$V_{PG(hyst)}$	FB PGOOD hysteresis voltage		15	28	45	mV
R_{PGOOD}	PGOOD pull-down resistance	V_{FB}=0V, I_{PGOOD}=5mA	--	50	--	Ω
$I_{PGOOD(lk)}$	PGOOD pin leakage current	V_{FB} = 600 mV, V_{PGOOD} = 5 V	--	--	20	uA
$t_{PGDELAY}$	PGOOD delay time after soft-start sequence is complete	Default settings	--	2	--	ms
SENSE						
Remote Sense Range			--	--	0.5	%Vo
UVLO						
$V_{IN(on)}$	Input turn-on voltage(1)	Default settings	--	6.25	--	V
$V_{IN(off)}$	Input turn-off voltage(1)	Default settings	--	6	--	V
$V_{INON(rng)}$	Programmable range for turn on voltage		4.25	--	14	V
$V_{INOFF(rng)}$	Programmable range for turn off voltage		4	--	13.75	V

(1) Hysteresis of at least 150 mV is specified by design.						
OUTPUT OVERVOLTAGE / UNDERVOLTAGE						
V_{FBOV}	FB pin over voltage threshold(1)	Default settings	--	800	--	mV
V_{FBUV}	FB pin under voltage threshold	Default settings	--	528	--	mV
$V_{UVOV(acc)}$	FB UV/OV accuracy over range		-4	--	4	%
(1) FB reference voltage is 600mV, if FB voltage reach 600mV, the product will turn off the drive, but the product will not enter the output over-voltage protection state (Latched) .						
CURRENT LIMIT						
$t_{OFF(oc)}$	Off-time between restart attempts	Hiccup mode	7 x t_{ss}			ms
$I_{OC(flt)}$	Output peak current over-current fault threshold	Default settings	--	50	--	A
		Programmable range	3	--	50	
$I_{OC(warn)}$	Output peak current over-current warning threshold	Default settings	--	49	--	A
		Programmable range	2	--	49	
$I_{OC(acc)}$	Output peak current over-current fault accuracy	IOUT = 40 A, IOUT_CAL_GAIN = 0.503 mΩ	-10	--	10	%
	Output peak current over-current warning accuracy	IOUT = 37 A, IOUT_CAL_GAIN = 0.503 mΩ	-10	--	10	
Short-circuit Protection		Default settings	Re-power on to recover			
TEMPERATURE SENSE AND THERMAL SHUTDOWN						
T_{SD}	P1 Junction shutdown temperature		--	160	--	℃
T_{HYST}	P1 Thermal shutdown hysteresis		--	20	--	℃
$T_{SNS(acc)}$	P3/P4 temperature sense accuracy(1)	–40℃ ≤ TSNS ≤ 125℃	-3	--	3	℃
$T_{OT(flt)}$	P3/P4 Over-temperature fault limit	Default settings	--	165	--	℃
	P3/P4 OT fault limit range		120	--	165	℃
$T_{OT(warn)}$	P3/P4 Over-temperature warning limit	Default settings	--	140	--	℃
	P3/P4 OT warning limit range		100	--	140	℃
$T_{OT(step)}$	P3/P4 OT fault/warning step		--	1	--	℃
$T_{OT(hys)}$	P3/P4 OT fault/warning hysteresis		--	20	--	℃
(1) Performance verified under application conditions. (2) P1, P2, P3, P4 defined at Definition of product operating Temperature.						
MEASUREMENT SYSTEM						

$M_{VOUT(rng)}$	VOUT measurement range		0.6	--	4.5	V
$M_{VOUT(acc)}$	VOUT measurement accuracy(2)	VOUT = 1V, 0℃ ≤ TJ ≤ 125℃	-0.8	--	0.8	%
$M_{IOUT(rng)}$	IOUT measurement range(1)		0	--	50	A
$M_{IOUT(acc)}$	IOUT measurement accuracy(2)	IOUT≥20 A, IOUT_CAL_GAIN = 0.503 mΩ, 0℃≤ TJ ≤ 125℃	-640	--	640	mA
(1) The actual measurement range is limited by IOUT_CAL_GAIN command. See the IOUT_CAL_GAIN (38h) section. (2) Performance verified under application conditions.						
CNTL						
V_{CNTL-H}	Input High Voltage		2.1	--	5	V
V_{CNTL-H}	Input Low Voltage		0	--	0.5	V
P_{CNTL}	Input standby power	Turned off with CNTL-pin	--	0.55	--	W
$t_{ON(dly)}$	Turn-on delay time	Default settings	--	0	--	ms
$t_{OFF(dly)}$	Turn-off delay time	Default settings	--	0	--	ms
PMBus INTERFACE						
V_{IH}	High-level input voltage, CLK, DATA		2.1	--	--	V
V_{IL}	Low-level input voltage, CLK, DATA		--	--	0.8	V
I_{IH}	High-level input current, CLK, DATA, CNTL	Pin voltage = 3.3 V	-10	--	10	uA
I_{IL}	Low-level input current, CLK, DATA, CNTL	Pin voltage = 0 V	-10	--	10	uA
V_{OL}	Low-level output voltage, DATA, SMBALRT	I_{OUT} = 4 mA	--	--	0.4	V
I_{OH}	High-level output open drain leakage current, DATA, SMBALRT		0	--	10	uA
I_{OL}	Low-level output open drain current, DATA, SMBALRT		4	--	--	mA
$C_{PIN-OUT}$	Pin capacitance, CLK, DATA		--	--	1	pF
f_{PMB}	PMBus operating frequency range	Slave mode	10	--	400	kHz
t_{BUF}	Bus free time between START and STOP		1.3	--	--	us
$t_{HD:STA}$	Hold time after repeated START		0.6	--	--	
$t_{SU:STA}$	Repeated START set-up time		0.6	--	--	
$t_{SU:STO}$	STOP setup time		0.6	--	--	
$t_{HD:DAT}$	Data hold time	Receive mode	0	--	--	ns
		Transmit mode	300	--	--	

$t_{SU:DAT}$	Data setup time		100	--	--	
$t_{TIMEOUT}$	Error signal / detect		25	--	35	ms
$t_{LOW:MEXT}$	Cumulative clock low master extend time		--	--	10	ms
$t_{LOW:SEXT}$	Cumulative clock low slave extend time		--	--	25	ms
t_{LOW}	Clock low time		1.3	--	--	us
t_{HIGH}	Clock high time		0.6	--	--	us
t_{FALL}	CLK/DATA fall time		--	--	300	ns
t_{RISE}	CLK/DATA rise time		--	--	300	ns
$t_{RETENTION}$	Retention of configuration parameters	TJ = 25℃	100	--	--	Year
Write_cycles	Number of nonvolatile erase/write cycles	TJ = 25℃	20	--	--	K cycle
External Capacitance						
C_{OUT-EX}	External Capacitance	ESR ≥ 0.15 mΩ	330	--	560	uF
		ESR ≥ 10 mΩ	660	--	15000	uf
MTBF						
MTBF			--	6015801	--	Hours
Mechanical Specifications						
WEIGHT			--	12	--	g
Dimensions			25.4 x 12.7 x 12.96 mm			
Cooling Method			Free air convection or forced convection			

Product Electrical Specification (Dual output)

Operating temperature is -40 to +85 ℃, V_{in} = 7.5 to 14.4 V, unless otherwise specified under Conditions.

Typical values given at: Operating temperature is +25 ℃, V_{in} = 12.0 V, max I_O, f=430 kHz, one output is enabled, unless otherwise specified under Conditions.

V_O defined by pin strap. Standard configuration.

Tested with external C_{IN} = 2x470 μF/10 mΩ OS-CON + 8 x 10 μF Ceramic, C_{OUT} =4 x 330 μF/10 mΩ Polymer + 10 x 100 uF Cemaric.

In the test set-up VSNS/GSNS lines are connected directly to load and all the output voltage measurements are made on output pins except line and load regulation.

Characteristics		Conditions	Min.	Typ.	Max.	Unit
INPUT VOLTAGE						
V_{in}	Input voltage		7.5	12	14.4	V
	Input voltage rise time	Monotonic	--	--	10	V/ms
OUTPUT VOLTAGE						
	Output voltage adjustment range		0.6	--	4.5	V
	Output voltage adjustment including PMBus margining		0.54	--	4.5	
	Output voltage set-point resolution		--	±0.025	--	%V_o
	Output voltage accuracy	1.0V≤Vo≤4.5V	-1	--	+1	%V_o
		Vo＜1.0V	-10	--	10	mV
	Line regulation	Vo = 0.6 V	--	1	--	mV
		Vo = 1.0 V	--	1	--	
		Vo = 1.8 V	--	2	--	
		Vo = 2.5 V	--	3	--	
		Vo = 3.3 V	--	3	--	
		Vo = 4.5 V	--	3	--	
	Load regulation	Vo = 0.6 V	--	1	--	
		Vo = 1.0 V	--	1	--	
		Vo = 1.8 V	--	2	--	
		Vo = 2.5 V	--	2	--	
		Vo = 3.3 V	--	2	--	
		Vo = 4.5 V	--	2	--	
V_{o-ac}	Output ripple & noise (up to 20 MHz bandwidth)	Vo = 0.6 V	--	7	--	mVp-p
		Vo = 1.0 V	--	8	--	
		Vo = 1.8 V	--	12	--	
		Vo = 2.5 V	--	14	--	
		Vo = 3.3 V	--	16	--	
		Vo = 4.5 V	--	19	--	
Temperature Coefficient		Operating temperature -40℃ to +85℃	--	±0.2	--	%/℃
Transient Response Deviation		Nominal input voltage, 50% load step change	--	30	--	mV
Transient Recovery Time			--	1	--	us
INPUT CURRENT						

$I_{in\text{-}no\ load}$	Input No Load Current	Vo = 0.6 Vdc	--	80	--	mA
		Vo = 4.5 Vdc	--	150	--	
I^2t	Inrush Transient		--	--	1	A^2s
OUTPUT CURRENT						
I_O	Output current (each output)	Vo = 0.6 V	0	--	30	A
		Vo = 1.0 V	0	--	30	A
		Vo = 1.8 V	0	--	30	A
		Vo = 2.5 V	0	--	30	A
		Vo = 3.3 V	0	--	27	A
		Vo = 4.5 V	0	--	20	A
I_{lim}	Current limit threshold (each output)	Test value with setting OCP threshold = 50 A	--	50	--	A
Efficiency						
η	Efficiency max I_O	Vo = 0.6 V	--	82	--	%
		Vo = 1.0 V	--	86	--	
		Vo = 1.8 V	--	90	--	
		Vo = 2.5 V	--	91	--	
		Vo = 3.3 V	--	92	--	
		Vo = 4.5 V	--	92	--	

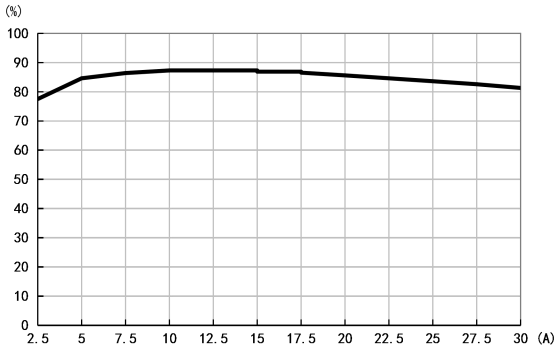
Typical Characteristic Curves (Dual output)

V_O = 0.6 V (Dual output)

Standard configuration unless otherwise specified, Operating temperature is+25℃, one output is enabled.

Efficiency

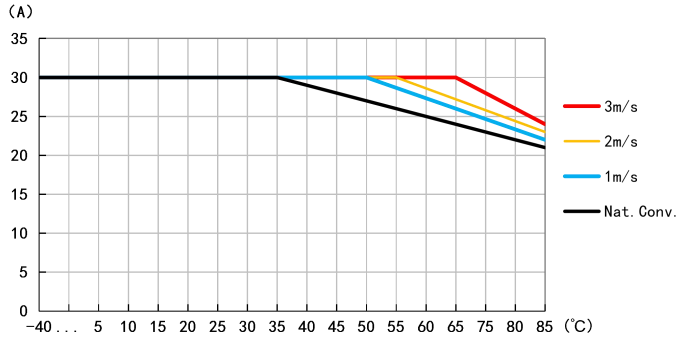
Efficiency vs. load current at V_{in} = 12 V.



Output Current Derating

Available load current vs. ambient air temperature and airflow at V_{in} = 12 V.

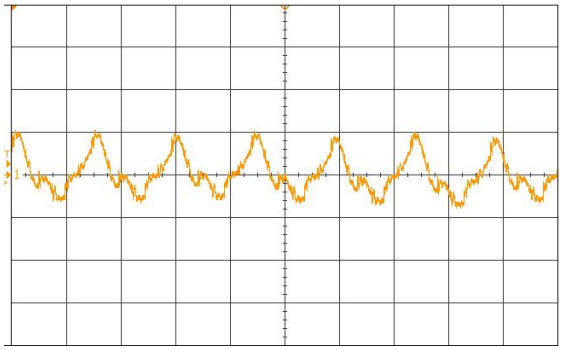
The other output is enabled at full load, the output voltage is set as 0.6 V.



Output Ripple and Noise

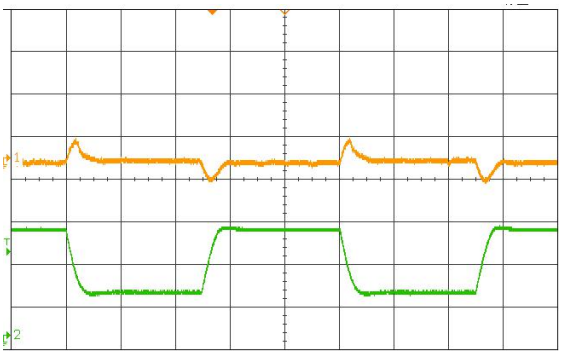
Fundamental output voltage ripple at V_{in} = 12 V, I_O = 30 A, C_{OUT} = 4 x 330 μF/10 mΩ + 10 x 100 μF

Scale: 5 mV/div, 2 μs/div, 20 MHz bandwidth.



Transient Response

Output voltage response to load current step change (25%–75%–25%) at V_{in} = 12 V, C_{OUT} = 4 x 330 μF/10 mΩ + 10 x 100 μF, di/dt = 2 A/μs, Scale from top: 50 mV/div, 10 A/div, 200 μs/div.



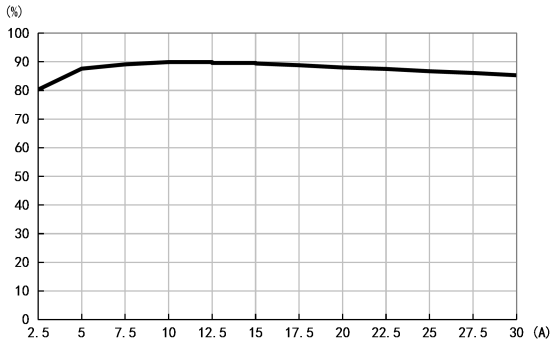
Typical Characteristic Curves (Dual output)

V_O = 1.0 V (Dual output)

Standard configuration unless otherwise specified, Operating temperature is+25℃, one output is enabled.

Efficiency

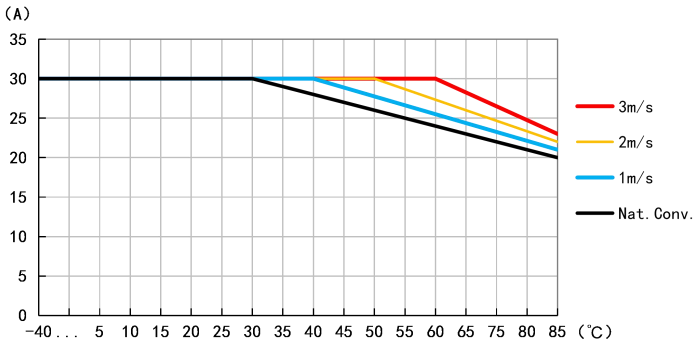
Efficiency vs. load current at V_{in} = 12 V.



Output Current Derating

Available load current vs. ambient air temperature and airflow at V_{in} = 12 V.

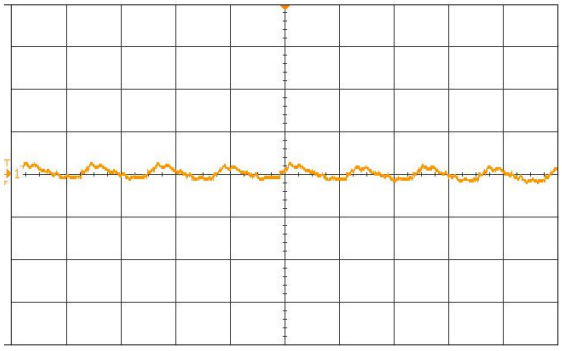
The other output is enabled at full load, the output voltage is set as 1.0 V.



Output Ripple and Noise

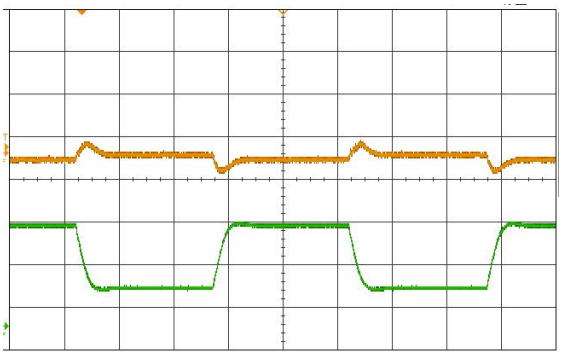
Fundamental output voltage ripple at V_{in} = 12 V, I_O = 30 A, C_{OUT} = 4 x 330 μF/10 mΩ + 10 x 100 μF

Scale: 10 mV/div, 2 μs/div, 20 MHz bandwidth.



Transient Response

Output voltage response to load current step change (25%–75%–25%) at V_{in} = 12 V, C_{OUT} = 4 x 330 μF/10 mΩ + 10 x 100 μF, di/dt = 2 A/μs, Scale from top: 50 mV/div, 10 A/div, 200 μs/div.



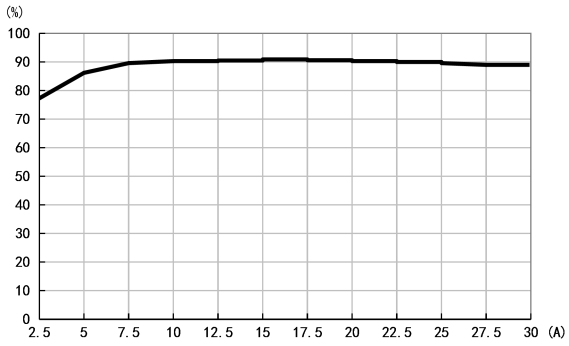
Typical Characteristic Curves (Dual output)

V_O = 1.8 V (Dual output)

Standard configuration unless otherwise specified, Operating temperature is+25℃, one output is enabled.

Efficiency

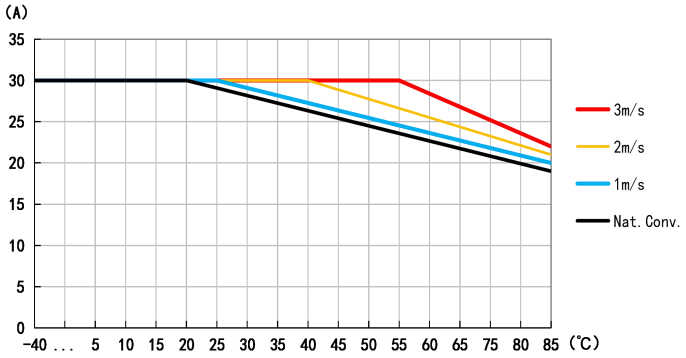
Efficiency vs. load current at V_{in} = 12 V.



Output Current Derating

Available load current vs. ambient air temperature and airflow at V_{in} = 12 V.

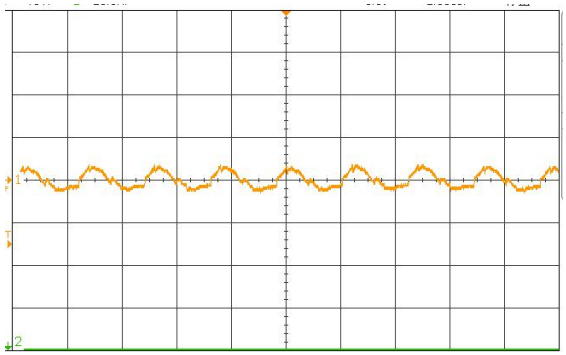
The other output is enabled at full load, the output voltage is set as 1.8 V.



Output Ripple and Noise

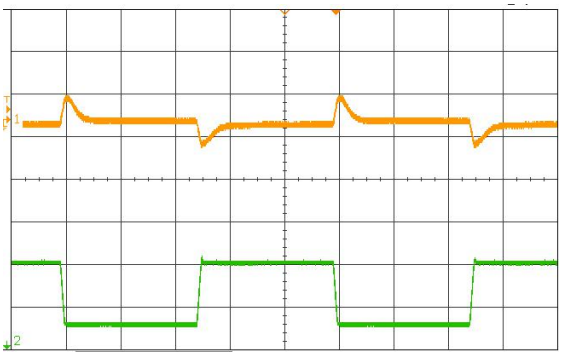
Fundamental output voltage ripple at V_{in} = 12 V, I_O = 30 A, C_{OUT} = 4 x 330 μF/10 mΩ + 10 x 100 μF

Scale: 10 mV/div, 2 μs/div, 20 MHz bandwidth.



Transient Response

Output voltage response to load current step change (25%–75%–25%) at V_{in} = 12 V, C_{OUT} = 4 x 330 μF/10 mΩ + 10 x 100 μF, di/dt = 2 A/μs, Scale from top: 50 mV/div, 10 A/div, 200 μs/div.



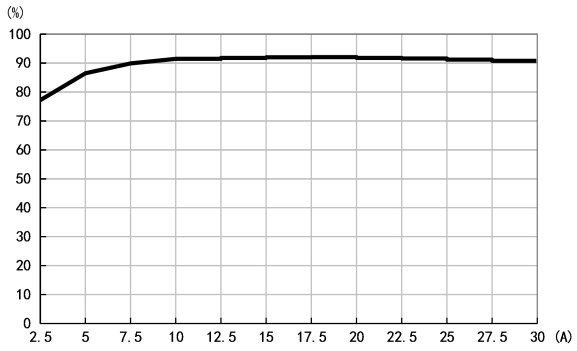
Typical Characteristic Curves (Dual output)

V_O = 2.5 V (Dual output)

Standard configuration unless otherwise specified, Operating temperature is+25℃, one output is enabled.

Efficiency

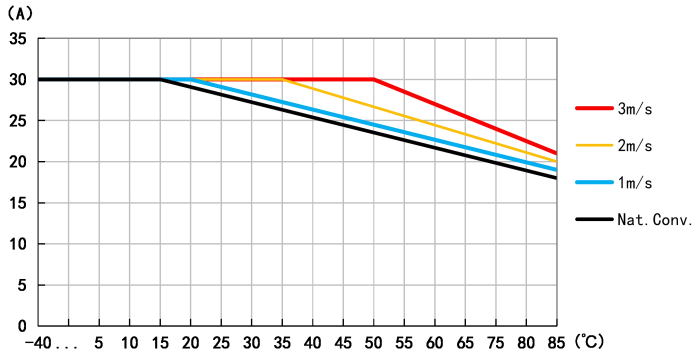
Efficiency vs. load current at V_{in} = 12 V.



Output Current Derating

Available load current vs. ambient air temperature and airflow at V_{in} = 12 V.

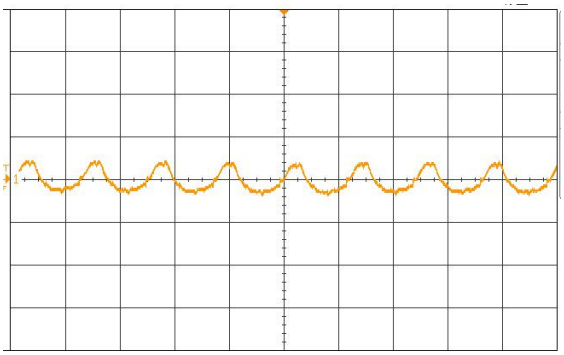
The other output is enabled at full load, the output voltage is set as 2.5 V.



Output Ripple and Noise

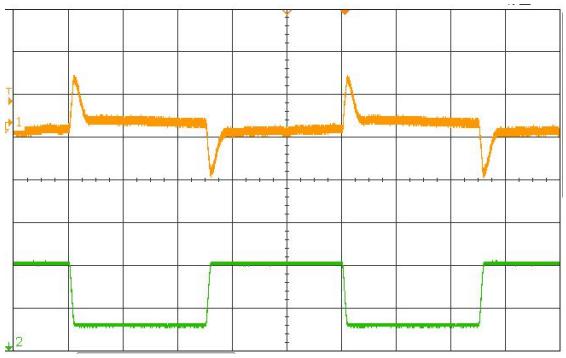
Fundamental output voltage ripple at V_{in} = 12 V, I_O = 30 A, C_{OUT} = 4 x 330 μF/10 mΩ + 10 x 100 μF

Scale: 10 mV/div, 2 μs/div, 20 MHz bandwidth.



Transient Response

Output voltage response to load current step change (25%–75%–25%) at V_{in} = 12 V, C_{OUT} = 4 x 330 μF/10 mΩ + 10 x 100 μF, di/dt = 2 A/μs, Scale from top: 50 mV/div, 10 A/div, 200 μs/div.



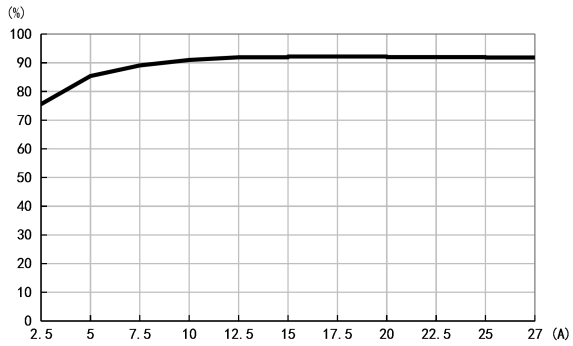
Typical Characteristic Curves (Dual output)

V_O = 3.3 V (Dual output)

Standard configuration unless otherwise specified, Operating temperature is+25℃, one output is enabled.

Efficiency

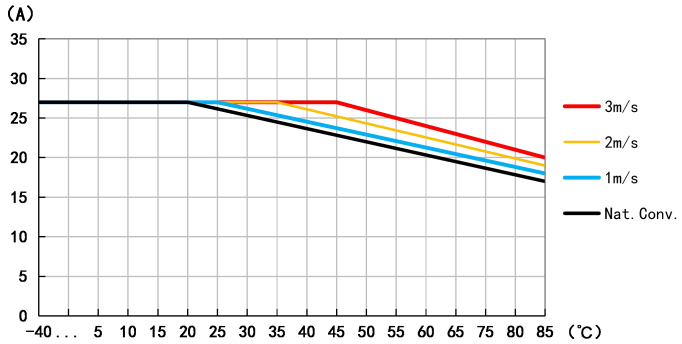
Efficiency vs. load current at V_{in} = 12 V.



Output Current Derating

Available load current vs. ambient air temperature and airflow at V_{in} = 12 V.

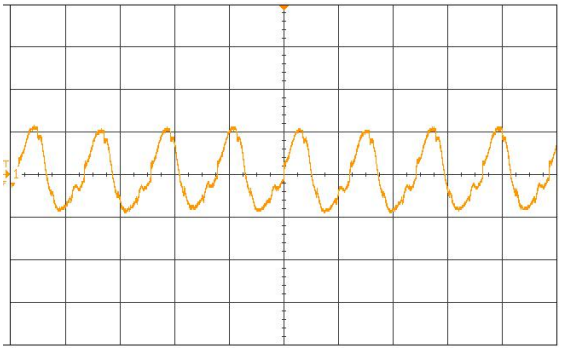
The other output is enabled at full load, the output voltage is set as 3.3 V.



Output Ripple and Noise

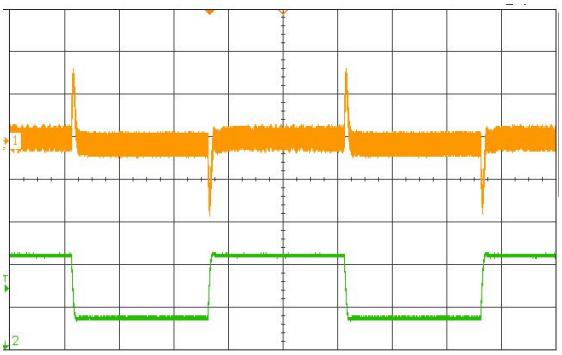
Fundamental output voltage ripple at V_{in} = 12 V, I_O = 27 A, C_{OUT} = 4 x 330 μF/10 mΩ + 10 x 100 μF

Scale: 5 mV/div, 2 μs/div, 20 MHz bandwidth.



Transient Response

Output voltage response to load current step change (25%–75%–25%) at V_{in} = 12 V, C_{OUT} = 4 x 330 μF/10 mΩ + 10 x 100 μF, di/dt = 2 A/μs, Scale from top: 20 mV/div, 10 A/div, 1000 μs/div.



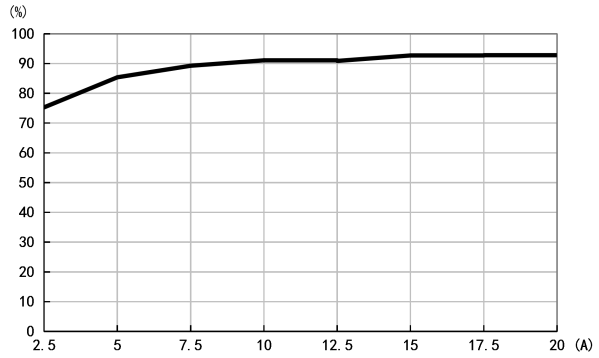
Typical Characteristic Curves (Dual output)

V_O = 4.5 V (Dual output)

Standard configuration unless otherwise specified, Operating temperature is+25℃, one output is enabled.

Efficiency

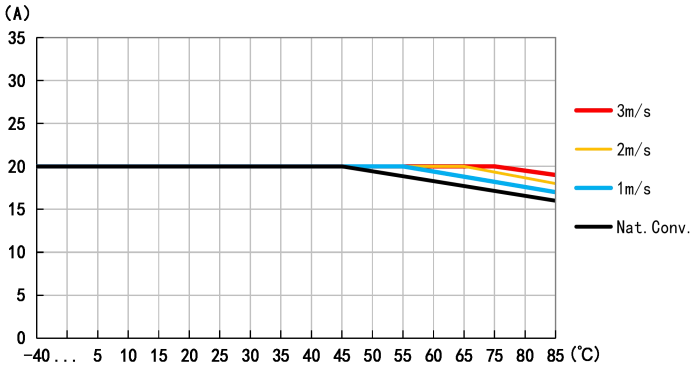
Efficiency vs. load current at V_{in} = 12 V.



Output Current Derating

Available load current vs. ambient air temperature and airflow at V_{in} = 12 V.

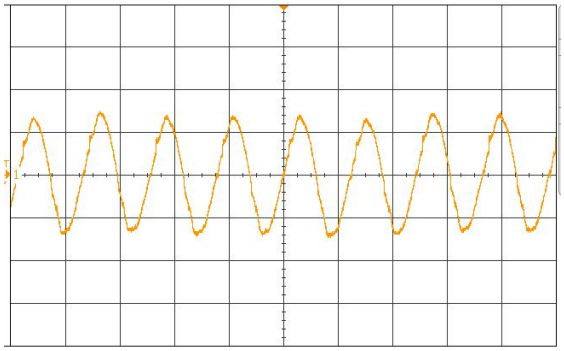
The other output is enabled at full load, the output voltage is set as 4.5 V.



Output Ripple and Noise

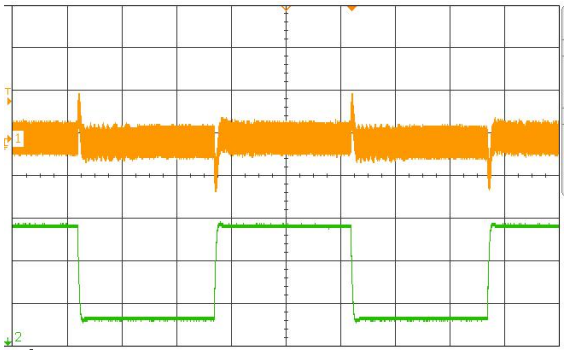
Fundamental output voltage ripple at V_{in} = 12 V, I_O = 20 A, C_{OUT} = 4 x 330 μF/10 mΩ + 10 x 100 μF

Scale: 5 mV/div, 2 μs/div, 20 MHz bandwidth.



Transient Response

Output voltage response to load current step change (25%–75%–25%) at V_{in} = 12 V, C_{OUT} = 4 x 330 μF/10 mΩ + 10 x 100 μF, di/dt = 2 A/μs, Scale from top: 20 mV/div, 5 A/div, 1000 μs/div.



Typical On/Off Characteristics (Dual output)

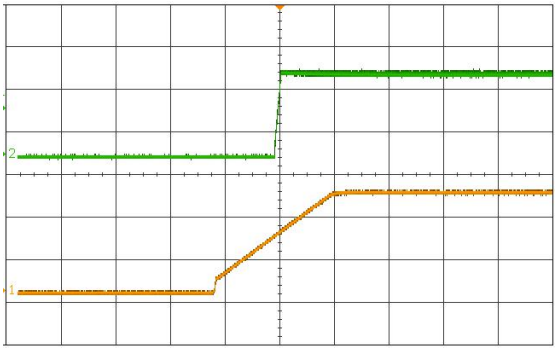
V_O = 1.0 V (Dual output)

Standard configuration, Operating temperature is +25 ℃, one output is enable.

Enable by input voltage

Output enabled by applying V_{in}. V_{in} = 12 V, I_O = 30 A.

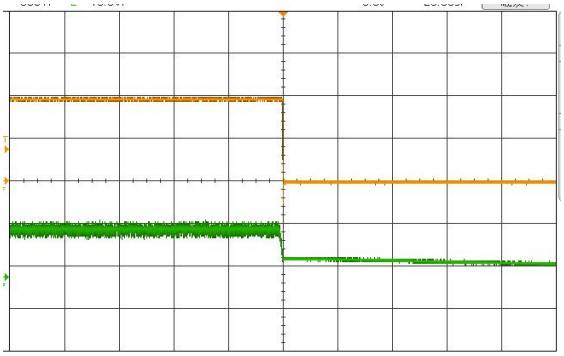
Scale from top: 0.5V/div（Vo）, 5 V/div（Vin）, 20 ms/div.



Disable by input voltage

Output disabled by removing V_{in}. V_{in} = 12 V, I_O = 30 A

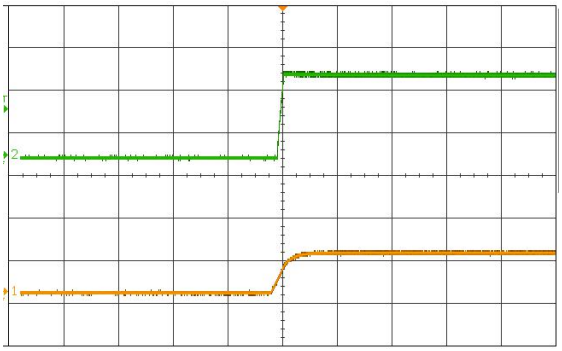
Scale from top: 0.5V/div（Vo）, 10 V/div（Vin）, 20 ms/div.



Enable by CNTL pin

Output enabled by CNTL pin. V_{in} = 12 V, I_O = 30 A.

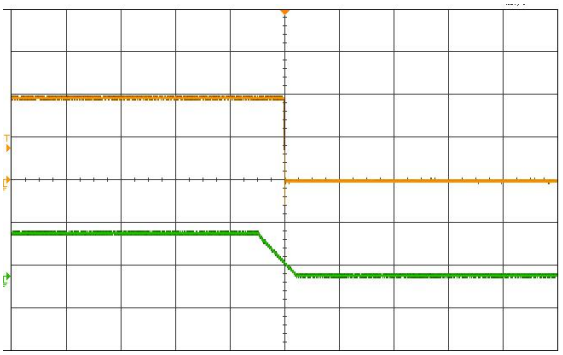
Scale from top: 0.5V/div（Vo）, 5 V/div（CNTL）, 20 ms/div.



Disable by CNTL pin

Output disabled by CNTL pin. V_{in} = 12 V, I_O = 30 A.

Scale from top: 0.5V/div（Vo）, 5 V/div（CNTL）, 20 ms/div.



Product Electrical Specification (Single output)

Operating temperature is -40 to +85 ℃, V_{in} = 7.5 to 14.4 V, unless otherwise specified under Conditions.

Typical values given at: Operating temperature is +25 ℃, V_{in} = 12.0 V, max I_O, f=430 kHz,unless otherwise specified under Conditions. V_O defined by pin strap. Standard configuration.

Tested with external C_{IN} = 2x470 μF/10 mΩ OS-CON + 10 x 10 μF Ceramic, C_{OUT} =8 x 330 μF/10 mΩ Polymer + 20 x 100 uF Cemaric.

In the test set-up VSNS/GSNS lines are connected directly to load and all the output voltage measurements are made on output pins except line and load regulation.

Characteristics		Conditions	Min.	Typ.	Max.	Unit
INPUT VOLTAGE						
V_{in}	Input voltage		7.5	12	14.4	V
	Input voltage rise time	Monotonic	--	--	10	V/ms
OUTPUT VOLTAGE						
	Output voltage adjustment range		0.6	--	4.5	V
	Output voltage adjustment including PMBus margining		0.54	--	4.5	V
	Output voltage set-point resolution		--	±0.025	--	%V_o
	Output voltage accuracy	Incl. line, load, temp, 1.0V≤Vo≤4.5V	-1	--	+1	%V_o
		Incl. line, load, temp, Vo＜1.0V	-10	--	10	mV
	Line regulation	Vo = 0.6 V	--	1	--	mV
		Vo = 1.0 V	--	2	--	
		Vo = 1.8 V	--	2	--	
		Vo = 2.5 V	--	3	--	
		Vo = 3.3 V	--	3	--	
		Vo = 4.5 V	--	3	--	
	Load regulation	Vo = 0.6 V	--	1	--	
		Vo = 1.0 V	--	1	--	
		Vo = 1.8 V	--	1	--	
		Vo = 2.5 V	--	2	--	
		Vo = 3.3 V	--	3	--	
		Vo = 4.5 V	--	3	--	
$V_{o\text{-}ac}$	Output ripple & noise (up to 20 MHz bandwidth)	Vo = 0.6 V	--	7	--	mVp-p
		Vo = 1.0 V	--	8	--	
		Vo = 1.8 V	--	12	--	
		Vo = 2.5 V	--	14	--	
		Vo = 3.3 V	--	16	--	
		Vo = 4.5 V	--	19	--	
Temperature Coefficient		Operating temperature -40℃ to +85℃	--	±0.2	--	%/℃
Transient Response Deviation		Nominal input voltage, 25% load step change	--	30	--	mV
Transient Recovery Time			--	1	--	us
INPUT CURRENT						

$I_{in\text{-}no\ load}$	Input No Load Current	Vo = 0.6 Vdc	--	160	--	mA
		Vo = 4.5 Vdc	--	300	--	mA
I^2t	Inrush Transient		--	--	1	A^2s
OUTPUT CURRENT						
I_O	Output current	Vo = 0.6 V	0	--	60	A
		Vo = 1.0 V	0	--	60	A
		Vo = 1.8 V	0	--	60	A
		Vo= 2.5 V	0	--	60	A
		Vo = 3.3 V	0	--	54	A
		Vo = 4.5 V	0	--	40	A
I_{lim}	Current limit threshold	Test value with setting OCP threshold = 50 A	--	100	--	A
Efficiency						
η	Efficiency max I_O	Vo = 0.6 V	--	82	--	%
		Vo = 1.0 V	--	86	--	
		Vo = 1.8 V	--	90	--	
		Vo = 2.5 V	--	91	--	
		Vo = 3.3 V	--	92	--	
		Vo= 4.5 V	--	92	--	

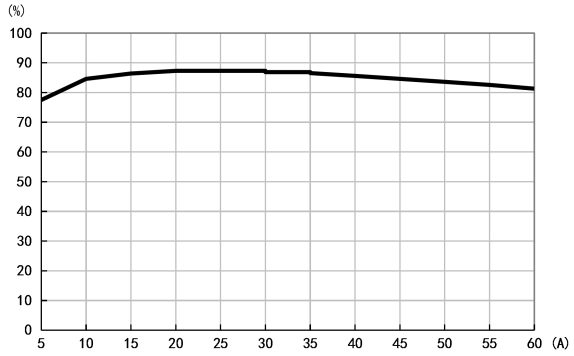
Typical Characteristic Curves (Signal output)

V_O = 0.6 V (Signal output)

Standard configuration unless otherwise specified, Operating temperature is+25℃

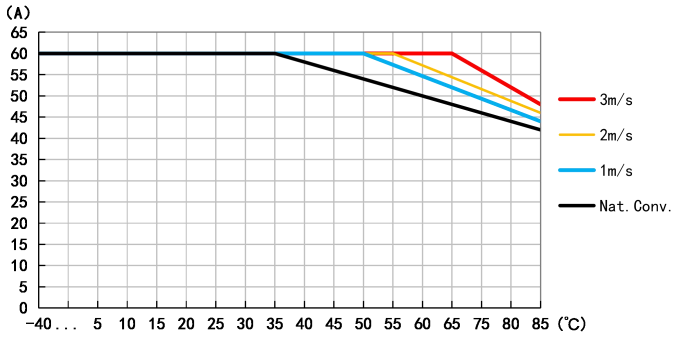
Efficiency

Efficiency vs. load current at V_{in} = 12 V



Output Current Derating

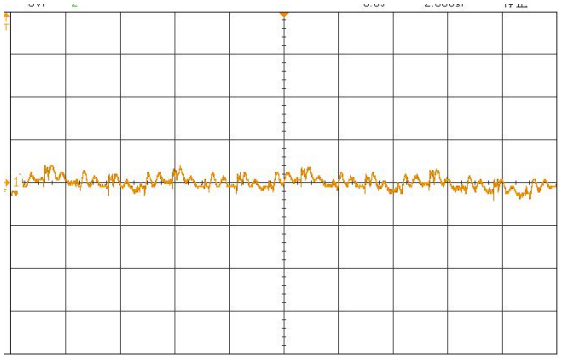
Available load current vs. ambient air temperature and airflow at V_{in} = 12 V.



Output Ripple and Noise

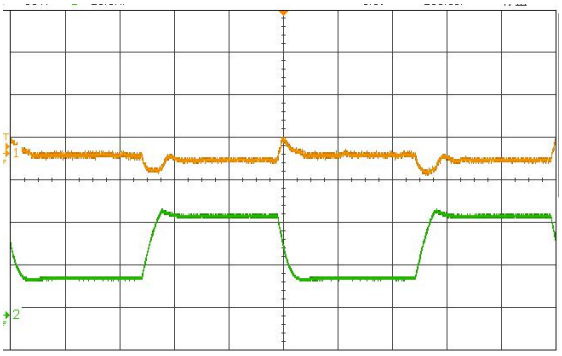
Fundamental output voltage ripple at V_{in} = 12 V, I_O = 60 A, C_{OUT} = 8 x 330 μF/10 mΩ + 20 x 100 μF

Scale: 5 mV/div, 2 μs/div, 20 MHz bandwidth.



Transient Response

Output voltage response to load current step change (25%–75%–25%) at V_{in} = 12 V, C_{OUT} = 8 x 330 μF/10 mΩ + 20 x 100 μF, di/dt = 2 A/μs, Scale from top: 50 mV/div, 20 A/div, 200 μs/div.



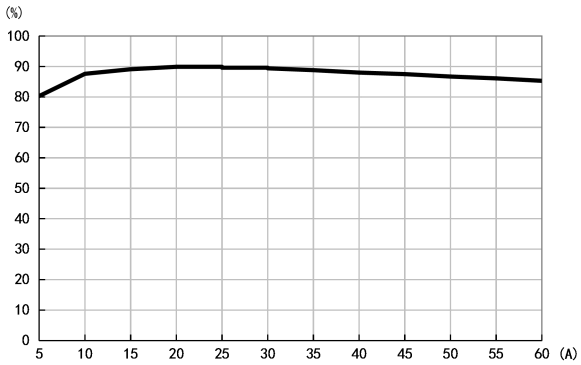
Typical Characteristic Curves (Signal output)

V_O = 1.0 V (Signal output)

Standard configuration unless otherwise specified, Operating temperature is+25℃.

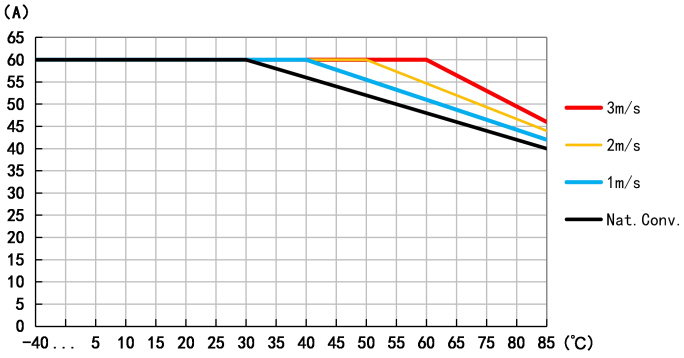
Efficiency

Efficiency vs. load current at V_{in} = 12 V.



Output Current Derating

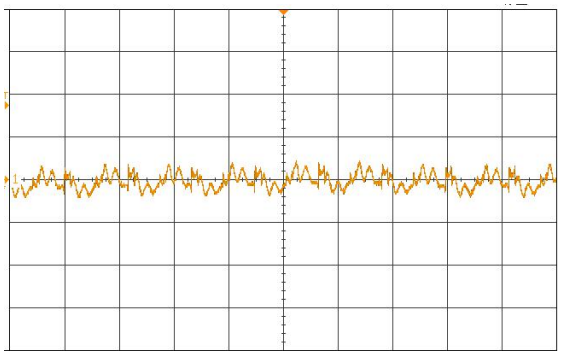
Available load current vs. ambient air temperature and airflow at V_{in} = 12 V.



Output Ripple and Noise

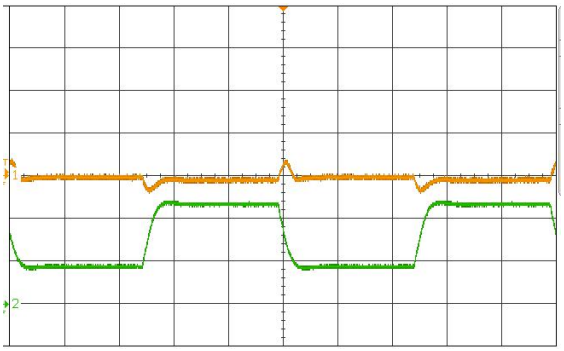
Fundamental output voltage ripple at V_{in} = 12 V, I_O = 60 A, C_{OUT} = 8 x 330 μF/10 mΩ + 20 x 100 μF

Scale: 5 mV/div, 2 μs/div, 20 MHz bandwidth.



Transient Response

Output voltage response to load current step change (25%–75%–25%) at V_{in} = 12 V, C_{OUT} = 8 x 330 μF/10 mΩ + 20 x 100 μF, di/dt = 2 A/μs, Scale from top: 50 mV/div, 20 A/div, 200 μs/div.



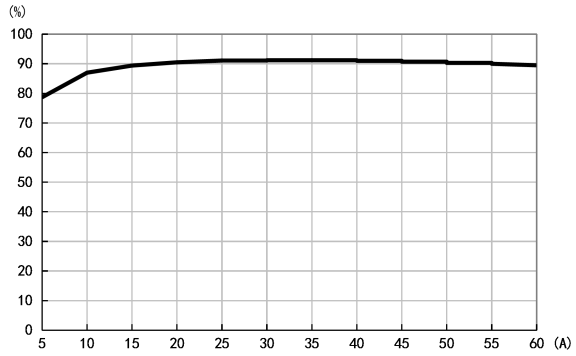
Typical Characteristic Curves (Signal output)

V_O = 1.8 V (Signal output)

Standard configuration unless otherwise specified, Operating temperature is+25℃.

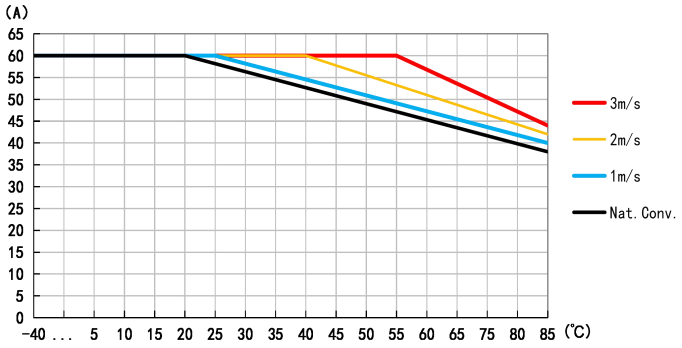
Efficiency

Efficiency vs. load current at V_{in} = 12 V.



Output Current Derating

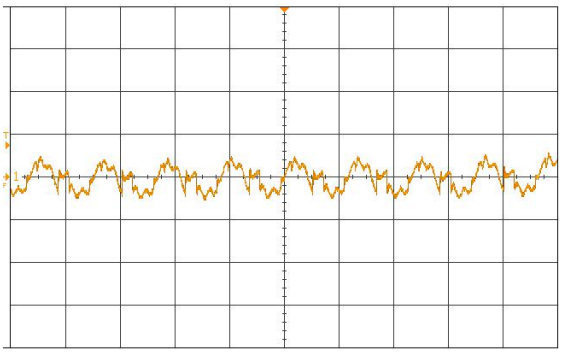
Available load current vs. ambient air temperature and airflow at V_{in} = 12 V.



Output Ripple and Noise

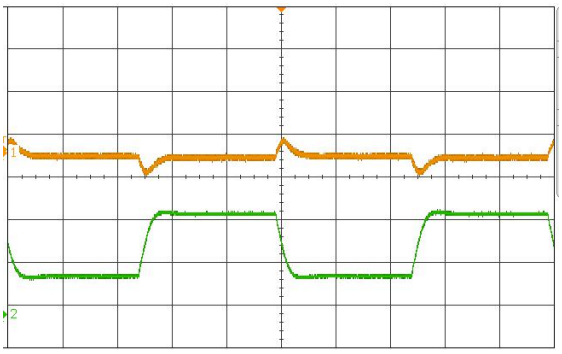
Fundamental output voltage ripple at V_{in} = 12 V, I_O = 60 A, C_{OUT} = 8 x 330 μF/10 mΩ + 20 x 100 μF

Scale: 5 mV/div, 2 μs/div, 20 MHz bandwidth.



Transient Response

Output voltage response to load current step change (25%–75%–25%) at V_{in} = 12 V, C_{OUT} = 8 x 330 μF/10 mΩ + 20 x 100 μF, di/dt = 2 A/μs, Scale from top: 50 mV/div, 20 A/div, 200 μs/div.



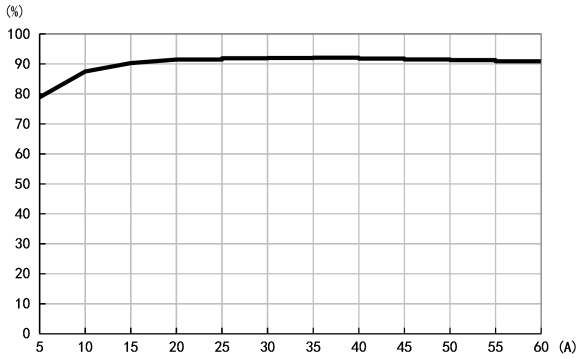
Typical Characteristic Curves (Signal output)

V_O = 2.5 V (Signal output)

Standard configuration unless otherwise specified, Operating temperature is+25℃.

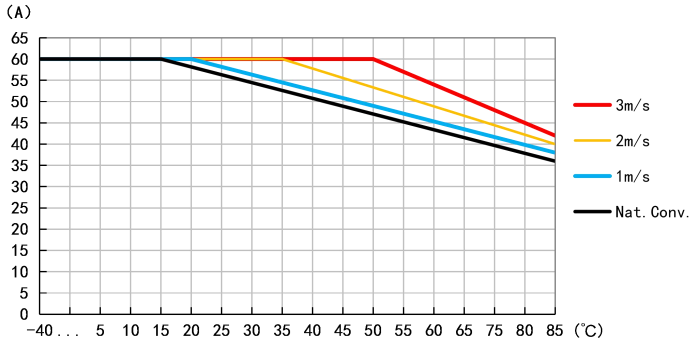
Efficiency

Efficiency vs. load current at V_{in} = 12 V.



Output Current Derating

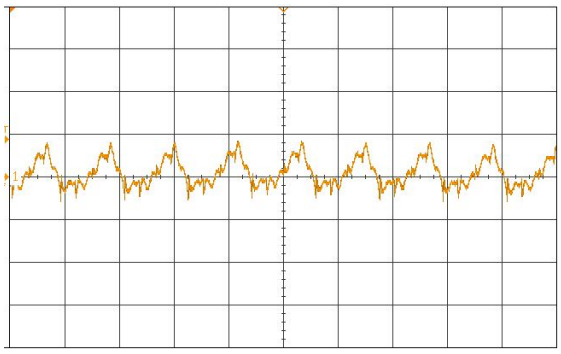
Available load current vs. ambient air temperature and airflow at V_{in} = 12 V.



Output Ripple and Noise

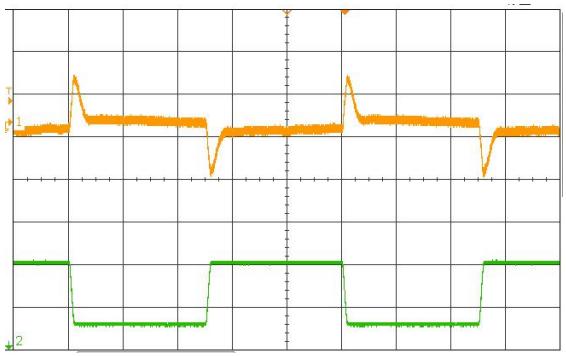
Fundamental output voltage ripple at V_{in} = 12 V, I_O = 60 A, C_{OUT} = 8 x 330 μF/10 mΩ + 20 x 100 μF

Scale: 5 mV/div, 2 μs/div, 20 MHz bandwidth.



Transient Response

Output voltage response to load current step change (25%–75%–25%) at V_{in} = 12 V, C_{OUT} = 8 x 330 μF/10 mΩ + 20 x 100 μF, di/dt = 2 A/μs, Scale from top: 50 mV/div, 20 A/div, 200 μs/div.



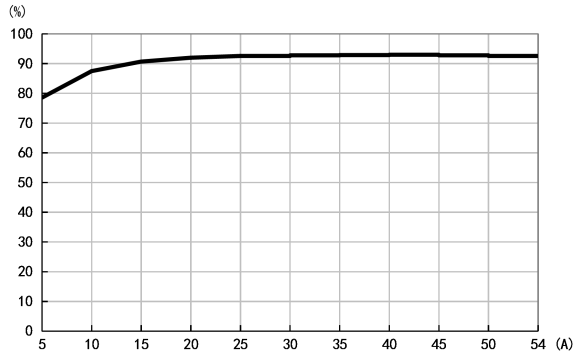
Typical Characteristic Curves (Signal output)

V_O = 3.3 V (Signal output)

Standard configuration unless otherwise specified, Operating temperature is+25℃.

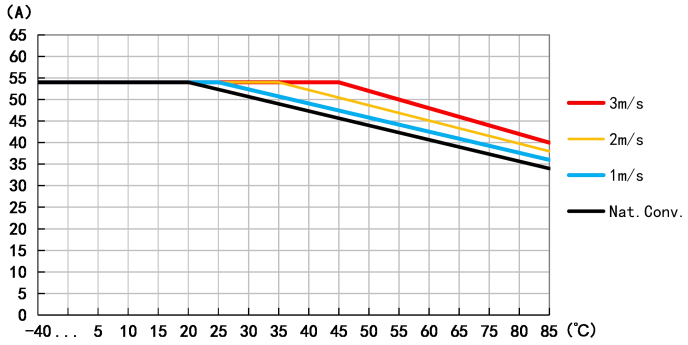
Efficiency

Efficiency vs. load current at V_{in} = 12 V.



Output Current Derating

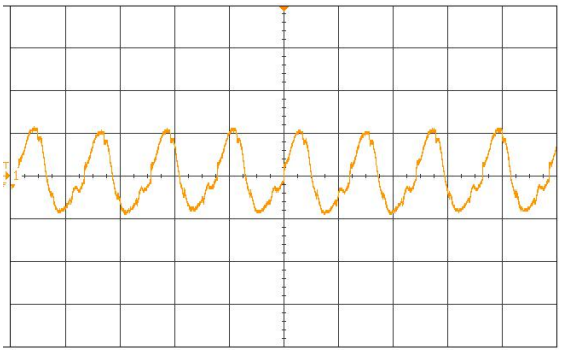
Available load current vs. ambient air temperature and airflow at V_{in} = 12 V.



Output Ripple and Noise

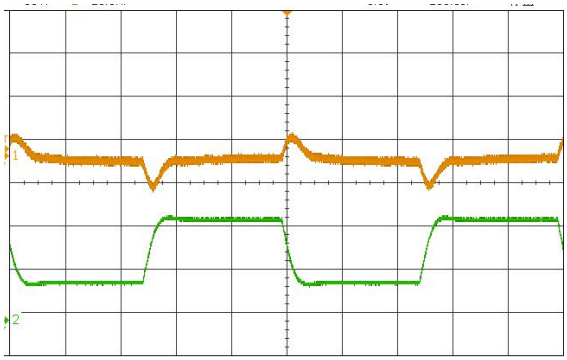
Fundamental output voltage ripple at V_{in} = 12 V, I_O = 54 A, C_{OUT} = 8 x 330 μF/10 mΩ + 20 x 100 μF

Scale: 5 mV/div, 2 μs/div, 20 MHz bandwidth.



Transient Response

Output voltage response to load current step change (25%–75%–25%) at V_{in} = 12 V, C_{OUT} = 8 x 330 μF/10 mΩ + 20 x 100 μF, di/dt = 2 A/μs, Scale from top: 50 mV/div, 20 A/div, 200 μs/div.



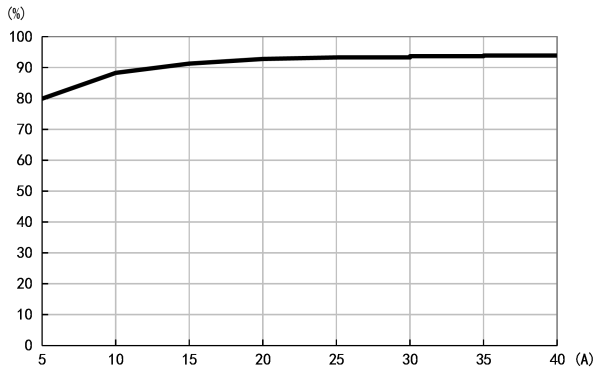
Typical Characteristic Curves (Signal output)

V_O = 4.5 V (Signal output)

Standard configuration unless otherwise specified, Operating temperature is+25℃.

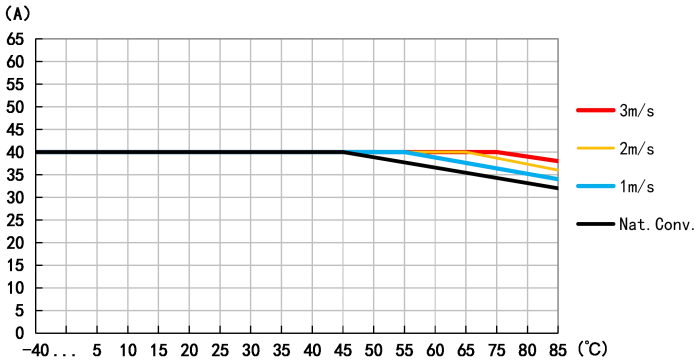
Efficiency

Efficiency vs. load current at V_{in} = 12 V.



Output Current Derating

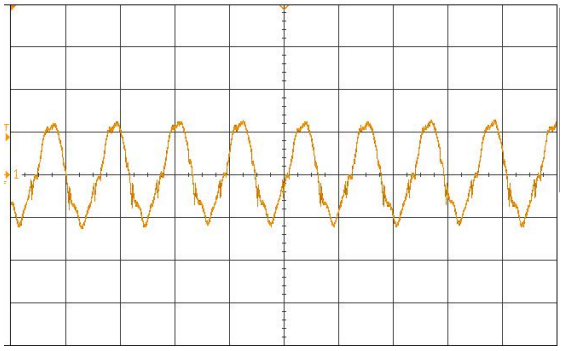
Available load current vs. ambient air temperature and airflow at V_{in} = 12 V.



Output Ripple and Noise

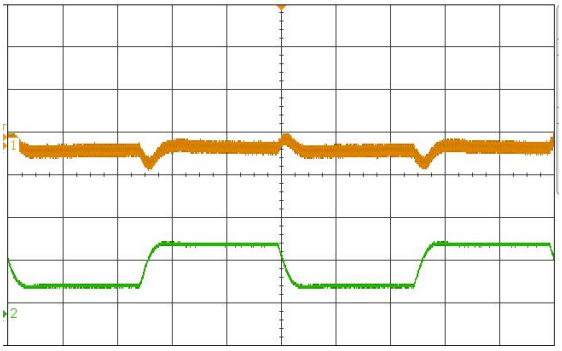
Fundamental output voltage ripple at V_{in} = 12 V, I_O = 40 A, C_{OUT} = 8 x 330 μF/10 mΩ + 20 x 100 μF

Scale: 5 mV/div, 2 μs/div, 20 MHz bandwidth.



Transient Response

Output voltage response to load current step change (25%–75%–25%) at V_{in} = 12 V, C_{OUT} = 8 x 330 μF/10 mΩ + 20 x 100 μF, di/dt = 2 A/μs, Scale from top: 50 mV/div, 20 A/div, 200 μs/div.



Typical On/Off Characteristics (Signal output)

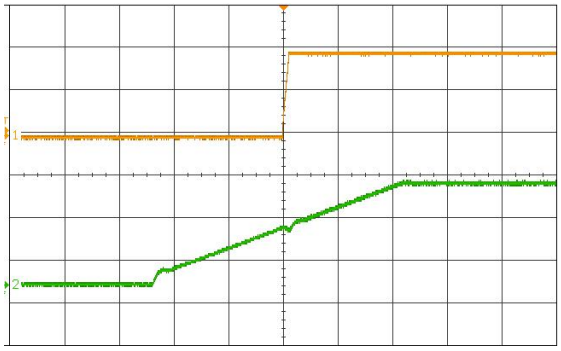
V_O = 1.0 V (Signal output)

Standard configuration, Operating temperature is +25 ℃.

Enable by input voltage – PG Push-Pull (default)

Output enabled by applying V_{in}. V_{in} = 12 V, I_O = 60 A.

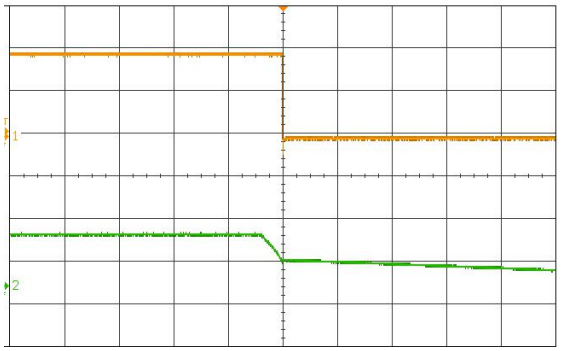
Scale from top: 0.5V/div（Vo）, 5 V/div（Vin）, 20 ms/div.



Disable by input voltage – PG Push-Pull (default)

Output disabled by removing V_{in}. V_{in} = 12 V, I_O = 60 A

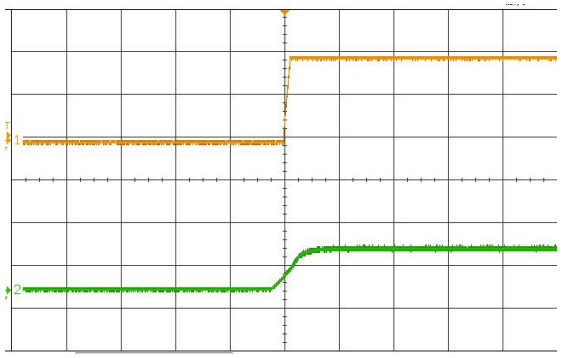
Scale from top: 0.5V/div（Vo）, 10 V/div（Vin）, 20 ms/div.



Enable by CNTL pin

Output enabled by CNTL pin. V_{in} = 12 V, I_O = 60 A.

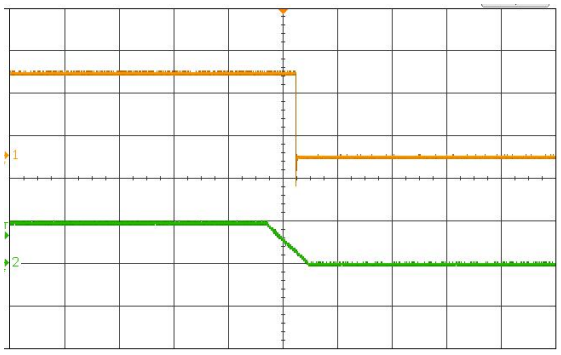
Scale from top: 0.5V/div（Vo）, 5 V/div（CNTL）, 20 ms/div.



Disable by CNTL pin

Output disabled by CNTL pin. V_{in} = 12 V, I_O = 60 A.

Scale from top: 0.5V/div（Vo）, 5 V/div（CNTL）, 20 ms/div.



PMbus Interface

PMBus General Description

Timing and electrical characteristics of the PMBus can be found in the PMB Power Management Protocol Specification, Part 1, revision 1.1 available at http://PMBus.org. The KD12T-60A device supports both the 100-kHz and 400-kHz bus timing requirements. The KD12T-60A device does not stretch pulses on the PMBus when communicating with the master device.

Communication over the KD12T-60A device PMBus interface can support the packet error checking (PEC) scheme if desired. If the master supplies CLK pulses for the PEC byte, PEC is used. If the CLK pulses are not present before a STOP, the PEC is not used.

The KD12T-60A device supports a subset of the commands in the PMBus 1.1 specification. Most of the controller parameters can be programmed using the PMBus and stored as defaults for later use. All commands that require data input or output use the literal format. The exponent of the data words is fixed at a reasonable value for the command and altering the exponent is not supported. Direct format data input or output is not supported by the KD12T-60A device. See the Supported PMBus Commands section for specific details.

The KD12T-60A device also supports the SMBALERT response protocol. The SMBALERT response protocol is a mechanism by which a slave (the KD12T-60A device) can alert the bus master that it wants to talk. The master processes this event and simultaneously accesses all slaves on the bus (that support the protocol) through the alert response address. Only the slave that caused the alert acknowledges this request. The host performs a modified receive byte operation to get the slave's address. At this point, the master can use the PMBus status commands to query the slave that caused the alert. For more information on the SMBus alert response protocol, see the System Management Bus (SMBus) specification.

The KD12T-60A device contains non-volatile memory that is used to store configuration settings and scale factors. The settings programmed into the device are not automatically saved into this non-volatile memory though. The STORE_USER_ALL command must be used to commit the current settings to non-volatile memory as device defaults. The settings that are capable of being stored in non-volatile memory are noted in their detailed descriptions.

PMBus Address

The PMBus specification requires that each device connected to the PMBus have a unique address on the bus. The KD12T-60A device has 64 possible addresses (0 through 63 in decimal) that can be assigned by connecting resistors from the ADDR0 and ADDR1 pins to AGND. The address is set in the form of two octal (0-7) digits, one digit for each pin. ADDR1 is the high-order digit an ADDR0 is the low-order digit.

During PMBus communication, the PMBus address of the KD12T-60A device is the concatenation of '0b'+ADDR1+ADDR0. The R/W bit of PMBus protocol is added at the end of address to make it net 8-bit wide.

The E96 series resistors suggested for each digit value are shown in:

DIGIT	RESISTANCE (kΩ)
0	8.45
1	16.2
2	25.5
3	37.4
4	54.9
5	84.5
6	133
7	200

The KD12T-60A also detects values that are out of range on the ADDR0 and ADDR1 pins. If either pin is detected as having an out of range resistance connected to it, the device continues to respond to PMBus commands, but at address 127, which is outside of the possible programmed addresses. It is possible but not recommended to use the device in this condition, especially if other KD12T-60A devices are present on the bus or if another device could possibly occupy the 127 address.

NOTE: Some addresses are reserved by SMBus specification and must not be used by or assigned to SMBus slave device. Refer to SMBus specification for more information.

PMBus Connections

The KD12T-60A device supports both the 100-kHz and 400-kHz bus speeds. Connection for the PMBus interface hould follow the High Power DC specifications given in section 3.1.3 on the System Management Bus (SMBus) Specification V2.0 for the 400-kHz bus speed or the Low Power DC specifications in section 3.1.2. The complete SMBus specification is available from the SMBus website, smbus.org.

PMBus Data Format

There are three data formats supported in PMBus form commands that require representation of a literal number as their argument (commands that set thresholds, voltages or report such). A compatible device needs to only support one of these formats. The KD12T-60A device supports the linear data format only for these commands. In this format, the data argument consists of two parts, a mantissa and an exponent. The number represented by this argument can be expressed as shown in:

$$Value = Mantissa \times 2^{exponent}$$

Operating Information

Input Undervoltage Lockout (UVLO)

The input UVLO turn-on and turn-off thresholds are set through PMBus using VIN_ON and VIN_OFF commands. These thresholds must be set for both controllers in 3-phase and 4-phase applications.

External Input Capacitors

The input ripple RMS current in a buck converter can be estimated to

$$I_{inputRMS} = I_{load}\sqrt{D(1-D)} \quad (\text{valid for } D<1, \text{single-phase})$$

$$I_{inputRMS} = I_{load}\sqrt{D(0.5-D)} \quad (\text{valid for } D<0.5, \text{two-phase})$$

Where I_{load} is the output load current and D is the duty cycle.

For most applications non-tantalum capacitors are preferred due to the robustness of such capacitors to accommodate high inrush currents of systems being powered from very low impedance sources. It is recommended to use a combination of ceramic capacitors and low-ESR electrolytic/polymer bulk capacitors. The low ESR of ceramic capacitors effectively limits the input ripple voltage level, while the bulk capacitance minimizes deviations in the input voltage at large load transients.

If several products are connected in a phase spreading setup the amount of input ripple current, and capacitance per product, can be reduced. As shown in the above formula.

Ceramic input capacitors must be placed closely and with low impedance connections to the VIN and GND pins in order to be effective.

External Output Capacitors

The output capacitor requirement depends on two considerations; output ripple voltage and load transient response. To achieve low ripple voltage, the output capacitor bank must have a low ESR value, which is achieved with ceramic output capacitors. A low ESR value is critical also for a small output voltage deviation during load transients. Designs with smaller load transients can use fewer capacitors and designs with more dynamic load content will require more load capacitors to achieve a small output deviation. Improved transient response can also be achieved by adjusting the settings of the control loop of the product. Adding output capacitance decreases loop band-width.

It is recommended to locate low ESR ceramic and low ESR electrolytic/polymer capacitors as close to the output & VSENS as possible, using several capacitors in parallel to lower the effective ESR. It is important to use low resistance and low inductance PCB layouts and cabling in order for capacitance to be effective.

Remote Sense

The product has remote sense to compensate for the voltage drops due to parasitic impedance between converter's output and a load. The sense traces should be laid out as a differentia pair and preferably be shielded by the PCB ground layer to reduce noise susceptibility.

Start-up and Shutdown

The start-up and shutdown function of the device is controlled by an operation command, control pin or input voltage. A turn on delay and turn-off delay can be added via PMBus commands.

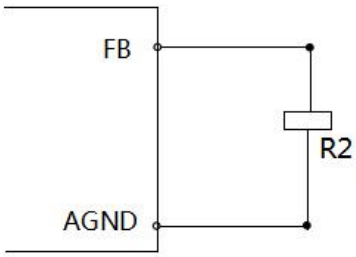
NOTE:

If the device turns off due to a turn-off delay time, any attempt to turn on the device before the turn-off delay time expires should be avoided. The device is available to be turned on only after the turn-off delay time expires and the device has been turned off.

For 3-phase and 4-phase configurations, the turn-on delay of both controllers must be programmed to the same value. The same requirement is for turn-off delay.

Output Voltage Adjustment

The 600-mV bandgap cell is internally connected to the non-inverting input of the error amplifier. The reference voltage is 600 mV with ±0.5% .



$$R2 = R_{FBX}(k\Omega) = \frac{6}{V_O - V_{FB}}$$

The nominal output voltage of the converter can be adjusted using the VREF_TRIM command See the MFR_SPECIFIC_04 (VREF_TRIM) (D4h) command description for the format of this command as used in the KD12T-60A device. The adjustment range is between –20% and 10% from the nominal output voltage. The VREF_TRIM command is typically used to trim the final output voltage of the converter. The resolution of the adjustment is 2 mV for each step. The nominal output for margining and VREF_TRIM remains limited to between –30% and 10%. Exceeding this range is not supported.

The KD12T-60A device operates in three states that determine the actual output voltage:

- No output margin

$$V_{FB} = VREF\_TRIM + 0.6$$

- Margin High Voltage State

$$V_{FB} = STEP\_VREF\_MARGIN\_HIGH + VREF\_TRIM + 0.6$$

- Margin Low State

$$V_{FB} = STEP\_VREF\_MARGIN\_LOW + VREF\_TRIM + 0.6$$

where

- VFB is the FB pin voltage
- VREF_TRIM is the offset voltage in volts to be applied to the output voltage
- VREF_MARGIN_HIGH is the requested margin high voltage
- VREF_MARGIN_LOW is the requested margin low voltage

Output Over-voltage/Under-voltage Protection

The KD12T-60A device monitors the voltage on FB pin to provide UV and OV protection. The UV threshold is proportional to the reference voltage. The OV threshold is a fixed value in factory default setting and can be a tracking value which is proportional to the reference voltage upon PMBus program.

The UV protection scheme is the same as OC protection scheme. When UV fault is triggered, both high-side and low-side MOSFETs are turned off. The IOUT_OC_FAULT_RESPONSE setting determines the controller response to UV fault. For example, if the IOUT_OC_FAULT_RESPONSE is set to restart the controller after OC fault, then the controller is internally also programmed to restart after a UV fault. UV protection is only detected after soft-start sequence has completed.

When an OV fault is triggered, the high-side MOSFET is turned off and the low-side MOSFET remains on to discharge the output. The controller keeps the low-side MOSFET on until VDD power recycle, CNTL pin or command toggling. This behavior protects the output against an overvoltage condition. When the OV threshold is a fixed value, OV protection is active at any time. When the OV threshold is proportional to the reference voltage, OV protection is enabled only after soft-start is done. When operating in multi-phase mode, only the FB pin of the master channel is detected for output voltage UV and OV fault. Output voltage related faults are not detected on any slave channels. Refer to the MFR_SPECIFIC_07 (PCT_VOUT_FAULT_PG_LIMIT) (D7h) and (E0h) MFR_SPECIFIC_16 (COMM_EEPROM_SPARE) sections for more information.

PGOOD Indication

The KD12T-60A device monitors the voltage on FB pin to indicate whether the output voltage is in regulation or not. During the soft-start sequence, the PG pin is pulled to GND. During operation using factory default settings, after the soft-start time expires, the PG pin releases after a 2-ms delay time if the output voltage is within the PGOOD window (between PG_Low and PG_High). The 2-ms delay can be disabled using the MFR_SPECIFIC_16 register. The PG pin is pulled to ground instantly when the output voltage is below PG_Low or above PG_High.

The PG_Low and PG_High value can be set by the PMBus command MFR_SPECIFIC_07 (PCT_VOUT_FAULT_PG_LIMIT).

Over-current Protection

The over-current protection uses a two-tier approach. Cycle-by-cycle current limit is implemented when the inductor peak current exceeds the set threshold. PMBus sets the current limit using the IOUT_OC_FAULT_LIMIT and IOUT_OC_WARN_LIMIT commands. After a series of seven OC counts, the device turns off both high-side and low-side MOSFETs and enters hiccup mode by default. Only cycle-by-cycle current limit is applied if OC is detected during soft-start operation.

The IOUT_OC_FAULT_RESPONSE PMBus command programs the response to an OC fault. The controller can be programmed to either shut down until power-cycle, CNTLx toggling, or to shut down and attempt restart after a delay of 7 x tON_RISE. When channel 2 is configured as a slave, this command cannot be programmed. In such a case where channel 2 is a slave, the fault response setting for channel 1 is automatically applied to channel 2. For 3-phase and 4-phase configurations, both the controllers must be programmed for the appropriate fault response.

Synchronization and PHSET

The switching frequency can be synchronized by an external clock on the SYNC pin. The frequency of the SYNC signal must be 4 times the switching frequency during 1-, 2-, or 4-phase operation, and must be 3 times the switching frequency during 3-phase operation. The SYNC signal must be a square waveform with 50% duty cycle. The high-level threshold must be above 2 V, and the low-level threshold must be below 0.8 V. The change on SYNC and PHSET setting occurs only after a power re-cycle.

In 3-phase and 4-phase applications, the device achieves clock and phase synchronization between the two controllers by connecting the SYNC pins and PHSET pins of the master controller to the corresponding pins on the slave controller. Phase configuration indicating number of phases is set according to the PMBus manufacturer specific command MFR_SPECIFIC_22 (E6h).

Soft-Start Time

The KD12T-60A device supports several soft-start times from 600 us to 9 ms selected by the TON_RISE PMBus command. See the command description for full details on the levels and implementation. When selecting the soft-start time, ensure that the charging current for the output capacitors is carefully considered. In some applications (for example, those with large amounts of output capacitance) this current can lead to problems with nuisance tripping of the overcurrent protection circuitry. To ensure that these problems do not happen, the output capacitor charging current should be included when considering where to set the overcurrent threshold. The output capacitor charging current can be found using Equation below:

$$I_{CAP} = \frac{V_{OUT} \times C_{OUT}}{t_{SS}}$$

where

- I_{CAP} is the startup charging current of the output capacitance in A
- V_{OUT} is the output voltage of the converter in V
- C_{OUT} is the total output capacitance in F
- t_{SS} is the selected soft-start time in seconds

With the charging current calculated, the overcurrent threshold can then be calibrated to the sum of the maximum load current and

the output capacitor charging current plus some margin. The amount of margin required depends on the individual application, but 25% is a suggested starting point. More or less may be required.

NOTE:

For 3-phase and 4-phase configurations, the soft-start time of both controllers must be programmed to the same value.

Turn-On/Turn-Off Delay and Sequencing

The KD12T-60A device provides many sequencing options. Using the ON_OFF_CONFIG command, each rail can be configured to start-up whenever the input is not in under-voltage lockout or to additionally require a signal on the CNTLx pin and/or receive an update to the OPERATION command over PMBus.

When the gating signal as specified by ON_OFF_CONFIG is reached for that rail, a programmable turn-on delay can be set with TON_DELAY. The rise time can be programmed with TON_RISE. When the specified signal (s) are set to turn the output off, a programmable turn-off delay set by TOFF_DELAY is used before switching is inhibited. More information can be found in the PMBus command descriptions.

When the output voltage is within the PGOOD limits after the start-up period, the PGOOD pin is asserted. This can be connected to the CNTL pin of another rail in dual-output mode or on another device to control turn-on and turn-off sequencing.

Current Sharing

All phases share the same comparator voltage (V_{COMP}). The sensed current in each phase is compared first in a current share block, then to an error current and fed into COMP. The resulting error voltage is compared with the voltage ramp to generate the PWM pulse.

Fault Communication

In the case of OC, VIN_UV, VOUT_UV, or OT fault, the FLT pin for the corresponding channel is pulled low internally. In addition, if the FLT pin of any channel is pulled low externally, that channel is shut down and both high-side and low-side MOSFETs are turned off. In 3-phase and 4-phase applications, the FLT pins of all phases of a rail must be connected together. Thus, a fault on any of the phases results in all the phases of that rail to shut down. If programmed to restart after fault, the rail restarts only after each phase on the rail has released the FLT pin.

FAULT	VIN UV	OC	VOUT UV	VOUT OV	OT	OTFI
Fault description	Vin voltage is above VIN_ON then drops below VIN_OFF	The MOS current is above OC fault threshold	FB voltage is below UV threshold.	FB voltage is below OV threshold.	The MOS temperature is above the OT threshold	The IC temperature is above junction shutdown threshold
Monitoring signal	Vin voltage	MOS current	FB voltage	FB voltage	MOS temperature	IC temperature
High-side MOSFET	OFF	OFF	OFF	OFF	OFF	OFF
Low-side MOSFET	OFF	OFF	OFF	ON	OFF	OFF
Hiccup/Latch	No	Determined by IOUT_OC_FAULT_RESPINSE	Determined by IOUT_OC_FAULT_RESPINSE	Latched	Hiccup after temperature below reset threshold	Hiccup after temperature below reset threshold
Before Soft-start	Enabled	Disabled	Disabled	Enabled at Fixed OV, Disabled at Tracking OV	Enabled	Enabled

During Soft-start	Enabled	Cycle-by-cycle limit	Disabled	Enabled at Fixed OV,Disabled at Tracking OV	Enabled	Enabled
After Soft-start	Enabled	Enabled	Enabled	Enabled	Enabled	Enabled

Device Functional Modes

The KD12T-60A device can be configured to operate in dual-output mode or 2-phase mode. It is also stack able up to four phases. Table lists the operating modes that are supported by the KD12T-60A device.

OPERATION MODE	LOCATION	CHANNEL	
Dual-output	Within a single device	CH1 = Master, CH2 = Master	
Two-phase	Within a single device	CH1 = Master, CH2 = Slave	
Three-phase	Between two devices	U1	CH1 = Master, CH2 = Slave2
		U2	CH1 = Slave1, CH2 = Independent
Four-phase	Between two devices	U1	CH1 = Master, CH2 = Slave2
		U2	CH1 = Slave1, CH2 = Slave3

The KD12T-60A device uses the remote sense amplifier of master channel to compensate for the parasitic offset to provide an accurate output voltage.

NOTE:

In multi-phase operation, FB pins of slave channels must be tied to the BP5 pin of the particular device. The COMP pins of all channels in the same rail are tied together, and ISH pins are tied together, to ensure current sharing between channels. FLT pins are tied together to ensure all channels in the same rail shut down in case a fault occurs on any channel. Ensure that the MFR_SPECIFIC_22 (PWM_OSC_SELECT) (E6h) command is set correctly, to ensure phase shift between phases.

In 3-phase and 4-phase operation, the SYNC pins of two devices are tied together, and PHSET pins of two devices are tied together to ensure phase shift between phases.

Over-temperature Fault Protection

The over-temperature fault and warning thresholds are programmable for the MOS temperature. In the case of an over-temperature fault, the detecting channel turns off both high-side and low-side MOSFETs. When the detected temperature cools to less than the turn-off hysteresis level, the channel attempts a restart. More information can be found in the OT_FAULT_LIMIT and OT_WARN_LIMIT command descriptions.

One on-chip temperature sensor monitors the device junction temperature. If the junction temperature of the device reaches the thermal shutdown limit (160℃ typical), the PWM output signals are turned off. When the junction temperature cools to the required level (140℃ typical), the PWM initiates soft-start as during a normal power-up cycle.

Thermal Consideration

The product is designed to operate in different thermal environments and sufficient cooling must be provided to ensure reliable operation. Cooling is achieved mainly by conduction, from the pins to the host board, and convection, which is dependent on the airflow across the product. Increased airflow enhances the cooling of the product.

The Output Current Derating graph found in the Output section for each model provides the available output current versus ambient air temperature and air velocity at specified Vin.

The product is tested on a 254 x 254 mm, 35 µm (1 oz) test board mounted vertically in a wind tunnel with a cross-section of 608 x 203 mm. The test board has 8 layers.

Note that the cooling via power pins does not only have to handle the power loss from the module. A low resistance between module

and target device is of major importance to reduce additional power loss.

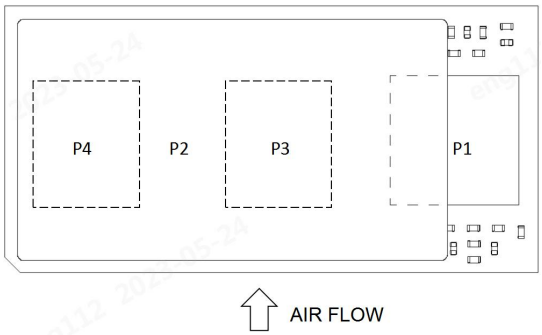
Definition of Product Operating Temperature

The surface temperature at positions P1, P2, P3 and P4 should not exceed the maximum temperatures in the table below. The number of measurement points may vary with different thermal design and topology. Temperatures above specified maximum measured at the specified positions are not allowed and may cause permanent damage.

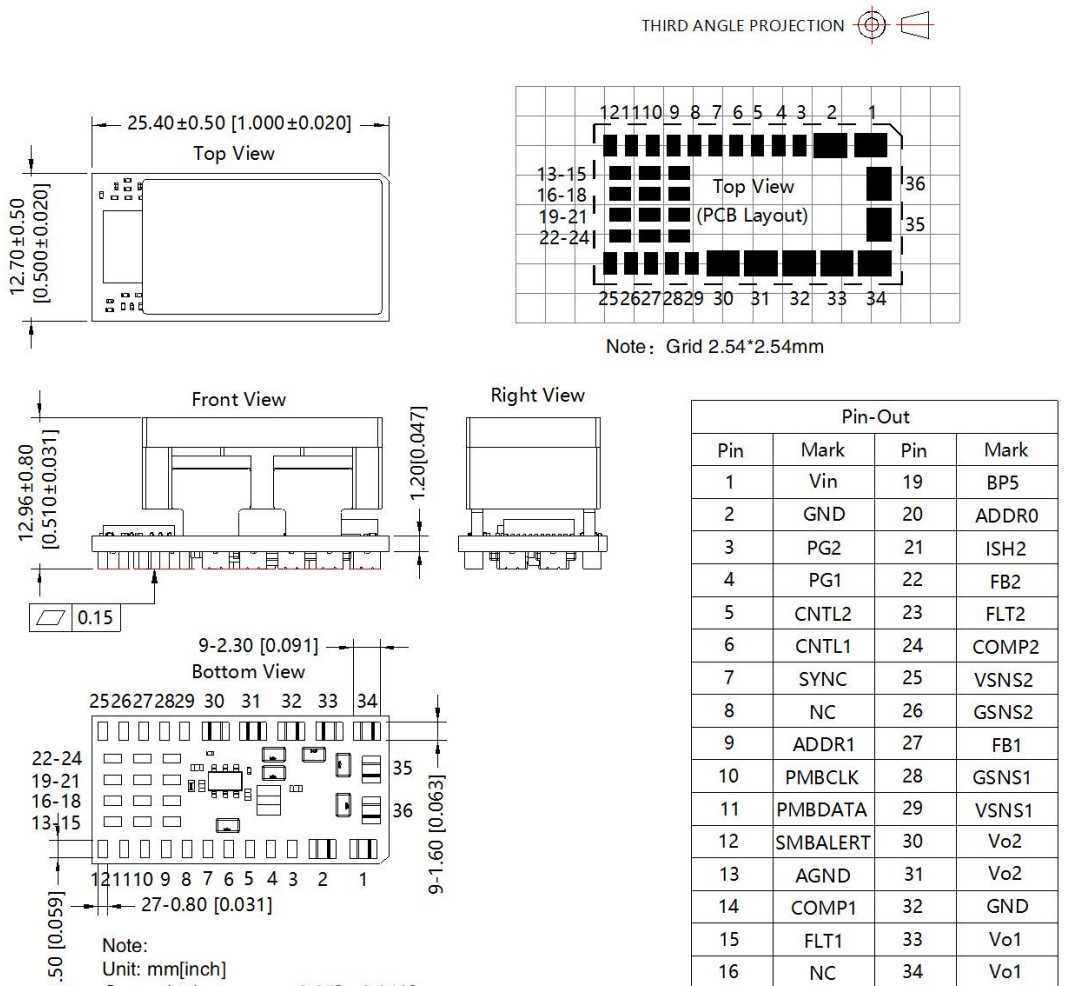
Position	Description	Max Temperature
P1	N1, Control circuit	T_{P1} = 130℃
P2	L1, Power inductor, Reference point	T_{P2} = 130℃
P3	N2, MOS Hot spot	T_{P3} = 130℃
P4	N3, MOS Hot spot	T_{P4} = 130℃

Since it is difficult to access positions P3 and P4, measuring the temperature at only position P2 is an alternative method to verify proper thermal conditions. If measuring only TP2 the maximum temperature of P2 must be lowered since typically TP1, TP3 and TP4 will be higher than TP2.

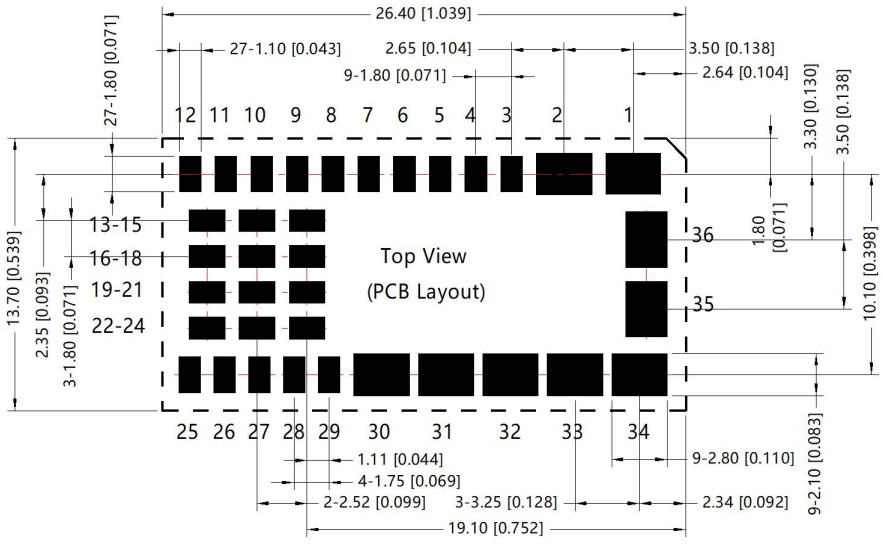
Using PMBUS command will get P1/P3/P4 temperature value.



Dimensions and Recommended Layout

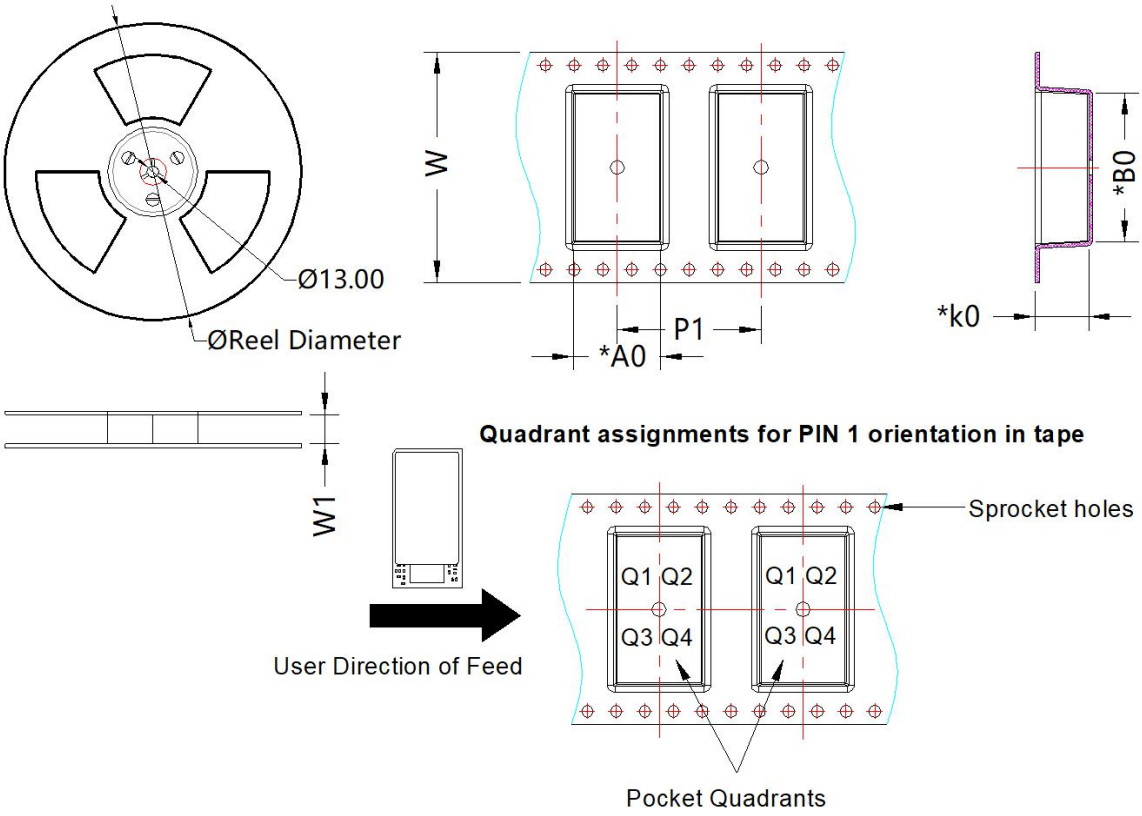


Pin-Out			
Pin	Mark	Pin	Mark
1	Vin	19	BP5
2	GND	20	ADDR0
3	PG2	21	ISH2
4	PG1	22	FB2
5	CNTL2	23	FLT2
6	CNTL1	24	COMP2
7	SYNC	25	VSNS2
8	NC	26	GSNS2
9	ADDR1	27	FB1
10	PMBCLK	28	GSNS1
11	PMBDATA	29	VSNS1
12	SMBALERT	30	Vo2
13	AGND	31	Vo2
14	COMP1	32	GND
15	FLT1	33	Vo1
16	NC	34	Vo1
17	PHSET	35	GND
18	ISH1	36	Vin



Scale 2：1

Packaging



Device	Package Type	Pin	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
KD12T-60A	SMD	36	160	330.0	44.4	14.08	26.58	14.26	24	44	Q1

PMBus Commands

CODE	COMMAND NAME	WORD/BYTE	DESCRIPTION: PMBus Command	USER WRITABLE	FACTORY DEFAULT VALUE
00h	PAGE	Byte	Locates separate PMBus command lists in multiple output environments	YES	0XXX XXX0
01h	OPERATION	Byte	Turn the unit on and off in conjunction with the input from the CONTROL pin. Set the output voltage to the upper or lower MARGIN VOLTAGES.	YES	0X00 00XX
02h	ON_OFF_CONFIG	Byte	Configures the combination of CONTROL pin input and serial bus commands needed to turn the unit on and off. This includes how the unit responds when power is applied.	YES	XXX1 0110
03h	CLEAR_FAULTS	Byte	Clears all fault status registers to 0x00. The "Unit is Off" bit in the status byte is not cleared when this command is issued.	YES[1]	NONE
10h	WRITE_PROTECT	Byte	Prevents unwanted writes to the device.	YES	000X XXXX
15h	STORE_USER_ALL	Byte	Saves the current configuration into the User Store. Note: This command writes to Non-Volatile Memory.	YES[1]	NONE
16h	RESTORE_USER_ALL	Byte	Restores Store. all parameters to the settings saved in the User	YES[1]	NONE
19h	CAPABILITY	Byte	PEC,SPD,ALRT	No	1011 0000
20h	VOUT_MODE	Byte	Read-Only Mode Indicator. The data format is linear with an exponent of -9	No	0001 0111
35h	VIN_ON	Word	Sets the value of the input voltage at which the unit should start power conversion	YES	1111 0000 0001 1001
36h	VIN_OFF	Word	Sets the value of the input voltage at which the unit should stop power conversion.	YES	1111 0000 0001 1000

38h	IOUT_CAL_GAIN	Word	Sets the ratio of the voltage at the current sense pins to the sensed current.	YES	1000 0000 0010 0001
39h	IOUT_CAL_OFFSET	Word	Nulls any offsets in the output current sensing circuit	YES	1110 0000 0000 0000
46h	IOUT_OC_FAULT_LIMIT	Word	Sets the value of the output current, in amperes, that causes the over-current detector to indicate an over-current fault condition.	YES	1111 1000 0110 0100
47h	IOUT_OC_FAULT_RESPONSE	Byte	Instructs the device on what action to take in response to an output over-current fault.	YES	0000 0111
4Ah	IOUT_OC_WARN_LIMIT	Word	Sets the value of the output current that causes an output Over-current warning	YES	1111 1000 0110 0010
4Fh	OT_FAULT_LIMIT	Word	Over temperature fault threshold	YES	0000 0000 1010 0101
5Ih	OT_WARN_LIMIT	Word	Over temperature warning threshold	YES	0000 0000 1000 1100
61h	TON_RISE	Word	Target soft-start rise time	YES	1110 0000 0010 1011
78h	STATUS_BYTE	Byte	Single byte status indicator	No	0x00 0000
79h	STATUS_WORD	Word	Full 2-byte status indicator	No	0000 0000 0x00 0000
7Ah	STATUS_VOUT	Byte	Output voltage fault status detail	No	0000 0000
7Bh	STATUS_IOUT	Byte	Output current fault status detail	No	0000 0000
7Dh	STATUS_TEMPERATURE	Byte	Temperature fault status detail	No	0000 0000
7Eh	STATUS_CML	Byte	Communication, memory, and logic fault status detail	No	0000 0000
80h	STATUS_MFR_SPECIFIC	Byte	Manufacturer specific fault status detail	No	0000 0000
8Bh	READ_VOUT	Word	Read output voltage	No	0000 0000 0000 0000
8Ch	READ_IOUT	Word	Read output current	No	1110 0000 0000 0000
8Eh	READ_TEMPERATURE_2	Word	Read off-chip temp sensor	No	1111 0000 0110 0100
98h	PMBUS_REVISION	Byte	PMBus Revision Information	No	0001 0001
D0h	MFR_SPECIFIC_00	Word	User scratch pad	YES	0000 0000 0000 0000
D4h	MFR_SPECIFIC_04	Word	VREF_TRIM	YES	0000 0000 0000 0000
D5h	MFR_SPECIFIC_05	Word	STEP_VREF_MARGIN_HIGH	YES	0000 0000 0001 1110
D6h	MFR_SPECIFIC_06	Word	STEP_VREF_MARGIN_LOW	YES	1111 1111 1110 0010

D7h	MFR_SPECIFIC_07	Byte	PCT_VOUT_FAULT_PG_LIMIT	YES	XXXX XX10
D8h	MFR_SPECIFIC_08	Byte	SWQUENCE_TON_TOFF_DELAY	YES	000X 000X
E0h	MFR_SPECIFIC_16	Word	COMM_EEPROM_SPARE	YES	1011 0001 xxxx x011
E5h	MFR_SPECIFIC_21	Word	IC options	YES	0111 1111 0000 0000
E6h	MFR_SPECIFIC_22	Word	PWM_OSC_SELECT	YES	0000 0000 0000 0000
E7h	MFR_SPECIFIC_23	Word	Paged and Common MASK_SMBALERT	YES	0000 0000 0000 0000
EFh	MFR_SPECIFIC_30	Word	Temperature offset	YES	1111 1000 0000 0000
FCh	MFR_SPECIFIC_44	Word	Device code, unique code to id part number	No	0000 0001 1110 0000

NOTE 1：No data bytes are sent, only the command code is sent.

PAGE (00h)

Format	Unsigned binary integer
Description	The PAGE command provides the ability to configure, control, and monitor through only one physical address both channels (outputs) of the device.
Default	0XXX XXX0 (binary)

PAGE							
r/w	r	r	r	r	r	r	r/w
7	6	5	4	3	2	1	0
PA	X	X	X	X	X	X	P0

Bits	Field Name	Description
7,0	PA,P0	00: (Default) All commands address the first channel. 01: All commands address the second channel. 10: Illegal input-ignore this write, take no action. 11: All commands address both channels. If PAGE = 11, any then read commands point to PAGE0 always.
6:1	X	X indicates writes are ignored and reads are 0. Any values written to read-only registers are ignored.

OPERATION (01h)

Format	Unsigned binary integer
Description	The OPERATION command is used to turn the device output on or off in conjunction with the input from the CNTLx pin (where x = 1 for channel 1 and x = 2 for channel 2). It is also used to set the output voltage to the upper or lower MARGIN levels. OPERATION is a paged register. In order to access OPERATION register for channel 1 of the device, PAGE must be set to 0. In order to access OPERATION register for channel 2 of the device, PAGE must be set to 1. For simultaneous access of channels 1 and 2, PAGE command must be set to 11. If the channel is configured as a SLAVE, this command can not be accessed for that channel. Any writes to the SLAVE channel for this command are ignored. An attempt to read and write the SLAVE channel command results in a NACK'd command and the reporting of an IVC fault and triggering of SMB_ALERT.
Default	0X0000XX (binary)

r/w	r	r/w	r/w	r/w	r/w	r	r
7	6	5	4	3	2	1	0
On	0	Margin				X	X

Bits	Field Name	Description
7	On	The On bit is used to enable to IC via PMBus. The necessary condition for this bit to be effective is that the cmd bit in the ON_OFF CONFIG register is set high. However, the cmd bit being high is not a sufficient condition to enable the IC via the On bit, as specified below: 0: (Default) The device output is not enabled via PMBus. 1: The device output is enabled if: a. The supply voltage VIN is greater than the VIN_UVLO threshold, the cmd bit is high, and b. The bit cpr in the ON_OFF CONFIG register is low, or c. The bit cpr is high and the CNTL_EN pin is enabled (high or low).
6	0	X: Default
5:2	Margin	If Margin Low is enabled, load the value from the STEP_VREF_MARGIN_LOW command. If Margin High is enabled, load the value from the STEP_VREF_MARGIN_HIGH command. (See PMBus specification for more information) 0000: (Default) Margin Off 0101: Margin Low (Ignore Fault) 0110: Margin Low (Act On Fault) 1001: Margin High (Ignore Fault) 1010: Margin High (Act On Fault) Note: Any values written to read-only registers are ignored.
1:0	X	XX: Default X indicates writes are ignored and reads are 0. Any values written to read-only registers are ignored.

ON_OFF_CONFIG (02h)

Format	Unsigned binary integer
Description	The ON_OFF_CONFIG command configures the combination of CONTROL pin input and serial bus commands needed to turn the unit on and off. ON_OFF_CONFIG is a paged register. In order to access this register for channel 1 of the device, PAGE must be set to 0. In order to access this register for channel 2 of the device , PAGE must be set to 1. For simultaneous access of channels 1 and 2, PAGE command must be set to 11.If the channel is configured as a SLAVE, this command can not be accessed for that channel. Any writes to the SLAVE channel for this command are ignored. An attempt to read and write the SLAVE channel command results in a NACK'd command and the reporting of an IVC fault and triggering of SMB_ALERT. However, note that page 0 (channel 1) fault status bits (and associated smbalert state) should be capable of being cleared by toggling CNTL1 pin even if channel 1 is a slave. If channel 2 is a slave, then CNTL2 pin is disabled but toggling the CNTL1 pin should also clear page 1 (channel 2) fault status bits and related smbalert state. (The is recommendation is to tie together CNTL1 pins of both devices in a multi-phase configuration).
Default	XXX10110 (binary) The default power-up state can be changed using the STORE_USER_ALL command.

			r/w^E	r/w^E	r/w^E	r/w^E	r
7	6	5	4	3	2	1	0
X	X	X	pu	cmd	cpr	pol	cpa

Bits	Field Name	Description
7:5	X	X indicates writes are ignored and reads are 0.
4	pu	(Format: binary) Sets the default to either operate any time power is present or for the on/off to be controlled by CONTROL pin and/or PMBus commands. This bit is used in conjunction with the 'cp', 'cmd', and 'on' bits to determine start up. 0: Device powers up any time power is present regardless of state of the CONTROL pin.

		1: (Default) Device does not power up until commanded by the CNTL_EN pin and/or OPERATION command as programmed in bits (3:0) of the ON_OFF_CONFIG register.
3	cmd	(Format: binary) The cmd bit controls how the device responds to commands received via the serial PMBus. This bit is used in conjunction with the 'cpr', 'pu', and 'on' bits to determine start up. 0: (Default) Device ignores the on bit in the OPERATION command. 1: Device responds to the on bit in the OPERATION command, as explained above.
2	cpr	(Format: binary) Set the CNTL_EN pin response. This bit is used in conjunction with the 'cmd', 'pu', and 'on' bits to determine start up. The cpr bit being high is a necessary but not sufficient condition to enable the IC via the CNTL_EN pin: 0: Device ignores the CNTL_EN pin, i.e., on/off is controlled only by the OPERATION command 1: (Default) The device output is enabled if: a. The supply voltage VIN is greater than the VIN_UVLO threshold, and the CNTL_EN pin is active (high or low), and b. The bit cmd in the ON_OFF CONFIG register is low, or c. The bit cmd is high and the bit on in the OPERATION register is high.
1	pol	(Format: binary) Polarity of the CONTROL pin 1: (Default) CONTROL pin is active high 0: CONTROL pin is active low To change this value, the user must change this value in the register, save it to the EEPROM and then reboot the device via power down for the new value to take effect.
0	cpa	(Format: binary) Sets CONTROL pin action when commanding the unit to turn off. 0: (Default) Use the programmed turn-off delay. Note: Any values written to read-only registers are ignored on write and returns a'0'when read.

CLEAR_FAULTS (03h)

Format	N/A
Description	CLEAR_FAULTS is a paged command. In order to issue this command for channel 1 of the device, PAGE must be set to 0. In order to issue this command for channel 2 of the device , PAGE must be set to 1. For simultaneous access of channels 1 and 2, PAGE command must be set to 11. The CLEAR_FAULTS command is used to clear any fault bits that have been set. This command simultaneously clears all bits in all status registers in the selected PAGE. At the same time, the device negates (clears, releases) its SMB_ALERT signal output if the device is asserting the SMB_ALERT signal. The CLEAR_FAULTS command does not cause a unit that has latched off for a fault condition to restart. If the fault is still present when the bit is cleared, the fault bit shall immediately be set again and the host notified by the usual means.

Bits	Field Name	Description
7:0		No data bytes are sent, only the command code is sent.

WRITE_PROTECT (10h)

Format	N/A
Description	The WRITE_PROTECT command is used to control writing to the PMBus device. The intent of this command is to provide protection against accidental changes. This command is not intended to provide protection against deliberate or malicious changes to a device's configuration or operation. All supported commands may have their parameters read, regardless of the WRITE_PROTECT settings. Note: Valid setting of WRITE_PROTECT(7:5) bits disables the RESTORE_USER_ALL command's ability to restore EEPROM data to protected PMBus Control/Status Registers (CSRs). However, an EEPROM (via the RESTORE_USER_ALL execution) restores the data to any registers the remain unprotected (either by a valid WRITE_PROTECT(7:5) setting, or by any invalid setting of these bits). No WRITE_PROTECT(7:5) bit setting affects the Reset-Restore operation. All registers having EEPROM support get updated. Likewise, STORE_USER_ALL command operation remains unaffected.
Default	000XXXXX (binary) The default power-up state can be changed using the STORE_USER_ALL command.

r/w^E	r/w^E	r/w^E					
7	6	5	4	3	2	1	0
bit7	bit6	bit5	X	X	X	X	X

Bits	Field Name	Description
7	bit7	(Format: binary) 0: (Default) See table below. 1: Disable all writes except for the WRITE_PROTECT command. (bit5 and bit6 must be 0 to be valid data)
6	Bit6	(Format: binary) 0: (Default) See table below. 1: Disable all writes except for the WRITE_PROTECT, OPERATION, and PAGE commands. (bit5 and bit7 must be 0 to be valid data)
5	Bit5	(Format: binary) 0: (Default) See table below. 1: Disable all writes except for the WRITE_PROTECT, OPERATION, PAGE, and ON_OFF_CONFIG commands. (bit6 and bit7 must be 0 to be valid data)
4:0	X	X indicates writes are ignored and reads are 0. Note: Any values written to read-only registers are ignored.
Invalid data written to WRITE_PROTECT(7:5) causes the cml bit in the STATUS_BYTE and the ivd bit in the STATUS_CML registers to be set. INVALID DATA ALSO RESULTS IN NO WRITE PROTECTION (WRITE_PROTECT = 00h)!		

Data Byte Value	Action
1000 0000	Disables all WRITES except to the WRITE_PROTECT command.
0100 0000	Disables all WRITES except to the WRITE_PROTECT, OPERATION, and PAGE commands.
0010 0000	Disables all WRITES except to the WRITE_PROTECT, OPERATION, PAGE, and ON_OFF_CONFIG commands.

STORE_USER_ALL (15h)

Format	N/A
Description	Store all of the current storable register settings in the EEPROM memory as the new defaults on power up. It is permitted to use the STORE_USER_ALL command while the device is operating. However, the device may be unresponsive during the write operation with unpredictable memory storage results. It is recommended to turn the device output off before issuing this command. EEPROM programming faults set the cml bit in the STATUS_BYTE and the oth bit in the STATUS_CML registers.

RESTORE_USER_ALL (16h)

Format	N/A
Description	Write EEPROM data to those registers which: (1) have EEPROM support, and; (2) are unprotected according to current setting of the WRITE_PROTECT(7:5) bits. It is permitted to use the RESTORE_USER_ALL command while the device is operating. However, the device may be unresponsive during the copy operation with unpredictable, undesirable or even catastrophic results. It is recommended to turn the device output off before issuing this command.

Bits	Field Name	Description
7:0		No data bytes are sent, only the command code is sent.

CAPABILITY (19h)

Format	N/A
Description	This command provides a way for a host system to determine some key capabilities of this PMBus device.
Default	10110000 (binary)

r	r	r	r	r	r	r	r
7	6	5	4	3	2	1	0
PEC	SPD		ALRT	Reserved			

Bits	Field Name	Description
7	PEC	(Format: binary) Packet Error Checking is supported. 1: Default Note: Any values written to read-only registers are ignored.
6:5	SPD	(Format: binary) Maximum supported bus speed is 400 kHz. 01: Default Note: Any values written to read-only registers are ignored.
4	ALRT	(Format: binary) This device does have a SMB_ALERT pin and does support the SMBus Alert Response Protocol. 1: Default Note: Any values written to read-only registers are ignored.

3:0	Reserved	Reserved bits. 0000: Default

VOUT_MODE (20h)

Format	N/A
Description	The PMBus specification dictates that the data word for the VOUT_MODE command is one byte that consists of a 3-bit Mode and 5-bit parameter, as shown below. If a host sends a VOUT_MODE writer command, the device rejects the VOUT_MODE command, declare a communication fault for invalid data and respond as described in PMBus specification II section 10.2.2.
Default	00010111 (binary)

r	r	r	r	r	r	r	r
7	6	5	4	3	2	1	0
Mode			Exponent				

Bits	Field Name	Description
7:5	Mode	(Format: binary) 000: (Default) Linear Format
4:0	Exponent	(Format: two's complement binary) 10111: (Default) Exponent value =–9 Note: Any values written to read-only registers are ignored.

VIN_ON (35h)

The VIN_ON command sets the value of the input voltage at which the unit should start power conversion assuming all other conditions are met.

Values written within the supported VIN range are mapped to the nearest supported increment.

The supported VIN_ON values are:

4.25	4.5	4.75	5	5.25	5.5	5.75
6	6.25 (default)	6.5	6.75	7	7.25	7.5
7.75	8	8.25	8.5	8.75	9	9.25
9.5	10	10.5	11	11.5	12	12.5
13	14	15	16			

Format	Linear
Description	Attempts to write values outside of the acceptable range are treated as invalid data–in effect, the cml bit in the STATUS_BYTE register and the ivd bit in the STATUS_CML register are set, and SMB_ALERT asserted. Additionally, the value of VIN_ON remains unchanged. Maintaining values within "acceptable range" also indicates that writes to VIN_ON should not attempt to set its value less than that of VIN_OFF.
Default	The default setting results in a real VIN_ON of 6.25 V The default power-up state can be changed using the STORE_USER commands.

r	r	r	r	r	r	r	r	r	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Exponent					Mantissa										

Bits	Field Name	Description
7:3	Exponent	(Format: two's complement) This is the exponent for the linear format. Default: 11110 (bin) –2 (dec) (equivalent LSB = 0.25 V) These default settings are not programmable. Note: Any values written to read-only registers are ignored.
2:0 7:0	Mantissa	(Format: two's complement) This is the Mantissa for the linear format. Default: 000 0001 1001 (bin) 17 (dec) (equivalent VIN_ON voltage = 6.25 V) Minimum: 000 0001 0001 (bin) 17 (dec) (equivalent VIN_ON voltage = 4.25 V) Maximum: 000 0100 0000 (bin) 64 (dec) (equivalent VIN_ON voltage = 16 V) Note: Any values written to read-only registers are ignored

VIN_OFF (36h)

The VIN_OFF command sets the value of the input voltage at which the unit should stop power conversion.

Values written within the supported VIN range are mapped to the nearest supported increment.

The supported VIN_ON values are:

4 (default)	4.25	4.5	4.75	5	5.25	5.5
5.75	6 (default)	6.25	6.5	6.75	7	7.25
7.5	7.75	8	8.25	8.5	8.75	9
9.25	9.75	10.25	10.75	11.25	11.75	12.25
12.75	13.75	14.75	15.75			

Format	Linear
Description	Attempts to write values outside of the acceptable range are treated as invalid data – in effect, the cml bit in the STATUS_BYTE register and the ivd bit in the STATUS_CML register are set, and SMB_ALERT asserted. Additionally, the value of VIN_OFF remains unchanged. Maintaining values within "acceptable range" also indicates that writes to VIN_OFF should not attempt to set its value equal to or higher than that of VIN_ON.
Default	The default setting results in a real VIN_OFF of 6 V The default power-up state can be changed using the STORE_USER commands.

r	r	r	r	r	r	r	r	r	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Exponent					Mantissa										

Bits	Field Name	Description
7:3	Exponent	(Format: two's complement) This is the exponent for the linear format.

		Default: 11110 (bin) –2 (dec) These default settings are not programmable. Note: Any values written to read-only registers are ignored
2:0 7:0	Mantissa	(Format: two's complement) This is the linear format Mantissa. Default: 000 0001 1000 (bin) 16 (dec) (equivalent VIN_OFF voltage = 6 V) Minimum: 000 0001 0000 (bin) 16 (dec) (equivalent VIN_OFF voltage = 4 V) Maximum: 000 0011 1111 (bin) 63 (dec) (equivalent VIN_OFF voltage = 15.75 V) Note: Any values written to read-only registers are ignored.

IOUT_CAL_GAIN (38h)

Format	Linear
Description	The IOUT_CAL_GAIN is the ratio of the voltage at the current sense element to the sensed current. The units are ohms. The effective current sense element is the DCR of the inductor. The default setting is 0.5 mΩ. The resolution is 15.26 μΩ. The range is 0.244 to 7.747 mΩ. The IOUT_CAL_GAIN needs to be set to 0.5 mΩ for correct current readout. With regards to multi-phase operation: The user can always write to PAGE 0 (channel 1), PAGE 1 (channel 2) can be written only if it is a master (in effect, the user can not write PAGE 1 if it is configured as a slave). In this case where PAGE 1 is a slave, the PAGE 0 value is used for PAGE1/channel 2. Additionally, for 3-phase or 4-phase mode, the second IC PAGE 0 slave must be programmed by the user to have the same limit value as the master in IC 1 (in effect, the burden is on the user and can not be enforced by the hardware). An attempt to write a PAGE 1 SLAVE channel command results in a NACK'd command and the reporting of an IVC fault and triggering of SMB_ALERT. IOUT_CAL_GAIN is a paged register. In order to access this register for channel 1 of the device, PAGE(7),(0) must be set to 00. In order to access this register for channel 2 of the device , PAGE(7),(0) must be set to 01. For simultaneous access of channels 1 and 2, PAGE(7),(0) command must be set to 11
Default	The default setting results in a real IOUT_CAL_GAIN of 0.5035 mΩ. The default power-up state can be changed using the STORE_USER commands.

r	r	r	r	r	r	r	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Exponent					Mantissa										

Bits	Field Name	Description
7:3	Exponent	(Format: two's complement) This is the exponent for the linear format. Default: 10000 (bin)–16 (dec) (15.26 μΩ) These default settings are not programmable. Note: Any values written to read-only registers are ignored.

2:0 7:0	Mantissa	(Format: two's complement) This is the linear format Mantissa. Default: 000 0010 0001 (bin) 32 (dec) (32x15.26 μΩ = 0.5035 mΩ) Minimum 016 (dec) = 16x15.26 μΩ = 0.244 mΩ Maximum 508 (dec) = 508x 15.26 μΩ = 7.747 mΩ Note: Any values written to read-only registers are ignored.

IOUT_CAL_OFFSET (39h)

Format	Linear
Description	The IOUT_CAL_OFFSET is used to compensate for offset errors in the READ_IOUT command, the IOUT_OC_FAULT_LIMIT command and the IOUT_OC_WARN_LIMIT command. The units are amps. The default setting is 0 A. The resolution is 62.5 mA. The range is 3.9375 A to -4 A. Values outside the valid range are not checked and become aliased into the valid range. For example, 1110 0100 0000 0001 has an expected value of–63.9375 A but results in 1110 0111 1111 0001 which is–3.9375 A. This change occurs because the read-only bits are fixed. The exponent is always –4 and the 5 msb bits of the mantissa are always equal to the sign bit. IOUT_CAL_OFFSET is a paged register. In order to access this register for channel 1 of the device, PAGE(7),(0) must be set to 00. In order to access this register for channel 2 of the controller, PAGE(7),(0) must be set to 01. For simultaneous access of channels 1 and 2, PAGE(7),(0) command must be set to 11. With regards to multi-phase operation: The user can always write to PAGE 0 (channel 1). PAGE 1 (channel 2) can be written only if it is a master (i.e. the user can not write PAGE 1 if it is configured as a slave). In this case where PAGE 1 is a slave, the PAGE0 value are used for PAGE1/channel 2. Additionally, for 3-phase or 4-phase mode, the second IC PAGE 0 slave must be programmed by the user to have the same limit value as the master in IC 1 (in effect, the burden is on the user and can not be enforced by the hardware). An attempt to write a PAGE 1 SLAVE channel command results in a NACK'd command and the reporting of an IVC fault and triggering of SMB_ALERT.
Default	The default power-up state can be changed using the STORE_USER commands.

r	r	r	r	r	r/w^E	r*	r*	r*	r*	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Exponent					Mantissa										

Bits	Field Name	Description
7:3	Exponent	(Format: two's complement) This is the exponent for the linear format. Default: 11100 (bin) –4 (dec) (lsb = 62.5 mA) These default settings are not programmable. Note: Any values written to read-only registers are ignored.
2:0 7:0	Mantissa	(Format: two's complement) This is the linear format Mantissa. This is the linear format Mantissa. Default: 0 (bin) 0 (dec) Bits 1:0, and 7:6 changes for sign extension but are not otherwise programmable Note: Any values written to read-only registers are ignored.

IOUT_OC_FAULT_LIMIT (46h)

Format	Literal
Description	The IOUT_OC_FAULT_LIMIT command sets the value of the output current, in amperes, that causes the overcurrent detector to indicate an over-current fault condition. The IOUT_OC_FAULT_LIMIT should always be set to equal to or greater than the IOUT_OC_WARN_LIMIT. Writing a value to IOUT_OC_FAULT_LIMIT less than IOUT_OC_WARN_LIMIT causes the device to set the 'cml' bit in the STATUS_BYTE register and the 'ivd' bit in the STATUS_CML registers and assert SMB_ALERT. IOUT_OC_FAULT_LIMIT is a paged register. In order to access this register for channel 1 of the device, PAGE must be set to 0. In order to access this register for channel 2 of the controller, PAGE must be set to 1. For simultaneous access of channels 1 and 2, PAGE command must be set to 11. With regards to multi-phase operation: The user can always write to PAGE 0 (channel 1). PAGE 1 (channel 2) can be written only if it is a master (in effect, the user can not write PAGE 1 if it is configured as a slave). In this case where PAGE 1 is a slave, the PAGE0 value is used for PAGE1/channel 2. Additionally, for 3-phase or 4-phase mode, the second IC PAGE 0 slave must be programmed by the user to have the same limit value as the master in IC 1 (in effect, the burden is on the user and can not be enforced by the hardware). An attempt to write a PAGE 1 SLAVE channel command results in a NACK'd command and the reporting of an IVC fault and triggering of SMB_ALERT.
Default	1111 1000 0110 0100 (binary) The default setting results in a real IOUT_OC_FAULT_LIMIT of 50 A. The default power-up state can be changed using the STORE_USER commands.

r	r	r	r	r	r	r	r	r	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Exponent					Mantissa										

Bits	Field Name	Description
7:3	Exponent	(Format: two's complement) This is the exponent for the linear format. Default: 11111 (bin) -1 (dec) (0.5 A) These default settings are not programmable. Note: Any values written to read-only registers are ignored.
2:0 7:0	Mantissa	(Format: two's complement) Default: 000 0110 0100 (bin) 100 (dec) (equivalent analog OC = 50 A) Minimum: 000 0000 0110 (bin) 6 (dec) (equivalent analog OC = 3 A) Maximum: 000 0110 0100 (bin) 100 (dec) (equivalent analog OC = 50 A) Note: Any values written to read-only registers are ignored.

IOUT_OC_FAULT_RESPONSE (47h)

Format	Unsigned binary
Description	The IOUT_OC_FAULT_RESPONSE command instructs the device on what action to take in response to an IOUT_OC_FAULT_LIMIT or a VOUT under-voltage (UV) fault. When an OC fault is triggered, the device also: • Sets the OCF bit in the STATUS_BYTE register

	• Sets the OCFW and OCF bits in the STATUS_WORD register • Sets the OCF and OCW bits in the STATUS_IOUT register • Asserts SMB_ALERT, and notifies the host as described in section 10.2.2 of the PMBus Specification.. Bits (2:0) are hard-wired to 0x7 (3'b111) to indicate the 7xSoft-start time delay units in response to an over current or Vout undervoltage fault. IOUT_OC_FAULT_RESPONSE is a paged register. In order to access this register for channel 1 of the device, PAGE must be set to 0. In order to access this register for channel 2 of the device , PAGE must be set to 1. For simultaneous access of channels 1 and 2, PAGE command must be set to 11. With regards to multi-phase operation: The user can always write to PAGE 0 (channel 1). PAGE 1 (channel 2) can be written only if it is a master (in effect, the user can not write PAGE 1 if it is configured as a slave). In this case where PAGE 1 is a slave, the PAGE0 value is used for PAGE1/channel 2. Additionally, for 3-phase or 4-phase mode, the second IC PAGE 0 slave must be programmed by the user to have the same limit value as the master in IC 1 (in effect, the burden is on the user and can not be enforced by the hardware). An attempt to write a PAGE 1 (channel 2) SLAVE channel command results in a NACK'd command and the reporting of an IVC fault and triggering of SMB_ALERT.
Default	00000111 (binary) The default power-up state can be changed using the STORE_USER commands.

r	r	r/wE	r/wE	r/wE	r	r	r
7	6	5	4	3	2	1	0
0	0	RS(2)	RS(1)	RS(0)	1	1	1

Bits	Field Name	Description
7:6	0	Default: XX (X indicates writes are ignored and reads are 0) Note: Any values written to read-only registers are ignored.
5:3	RS(2:0)	(Format: binary) Output over current retry setting 000: (Default) A zero value for the Retry Setting indicates that the unit does not attempt to restart. The output remains disabled until the fault is cleared (See section 10.7 of the PMBus spec.). 111: A one value for the Retry Setting indicates that the unit goes through a normal startup (Wait → SoftStart) continuously, without limitation, until it is commanded off or bias power is removed or another fault condition causes the unit to shutdown. Any value other than 000 or 111 is not accepted, such and attempt causes the cml bit in the STATUS_BYTE register and the ivd bit in the STATUS_CML register to be set, and SMB_ALERT to be asserted.
2:0	1	Default: xxx (x indicates writes are ignored and reads are 1) Note: Any values written to read-only registers are ignored.

IOUT_OC_WARN_LIMIT (4Ah)

Format	Literal (5-bit two's complement exponent, 11-bit two's complement mantissa)
Description	The IOUT_OC_WARN_LIMIT command sets the value of the output current, in amperes, that causes the over-current

	detector to indicate an over-current warning condition by setting the OCW in bit-5 of the STATUS_IOUT register. • Sets the OTHER bit in the STATUS_BYTE register • Sets the OCFW bit in the STATUS_WORD register • Set the OCW bit in the STATUS_IOUT register • Notifies the host (Asserts SMB_ALERT) IOUT_OC_WARN_LIMIT is a paged register. In order to access this register for channel 1 of the K12DT-60A device, PAGE must be set to 0. In order to access this register for channel 2 of the K12DT-60A controller, PAGE must be set to 1. For simultaneous access of channels 1 and 2, PAGE command must be set to 11. With regards to multi-phase operation: PAGE 0 can always be written to. PAGE 1 can be written only if it is a master (in effect, you can not write PAGE 1 if it is configured as a slave). In this case where PAGE 1 is a slave, the PAGE0 value is used for PAGE1/channel 2. Additionally, for 3-phase or 4-phase mode, the second IC PAGE 0 slave must be programmed by the user to have the same limit value as the master in IC 1 (in effect, the burden is on the user and can not be enforced by the hardware). An attempt to write a PAGE 1 SLAVE channel command results in a NACK'd command and the reporting of an IVC fault and triggering of SMB_ALERT. The IOUT_OC_WARN_LIMIT should always be set to less than or equal to the IOUT_OC_FAULT_LIMIT. Writing a value to IOUT_OC_WARN_LIMIT greater than IOUT_OC_FAULT_LIMIT causes the device to set the cml bit in the STATUS_BYTE register and the ivd bit in the STATUS_CML registers and assert SMB_ALERT.
Default	1111 1000 0110 0010 (binary) The default setting results in a real IOUT_OC_WARN_LIMIT of 49 A. The default power-up state can be changed using the STORE_USER commands.

r	r	r	r	r	r	r	r	r	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Exponent					Mantissa										

Bits	Field Name	Description
7:3	Exponent	(Format: two's complement) This is the exponent for the linear format. Default: 11111 (bin) –1 (dec) (0.5 A) These default settings are not programmable. Note: Any values written to read-only registers are ignored.
2:0 7:0	Mantissa	(Format: two's complement) This is the Mantissa for the linear format. Output over current retry setting Default: 000 0110 0010 (bin) 98 (dec) (equivalent analog OC = 49 A) Minimum: 000 0000 0100 (bin) 4 (dec) (equivalent analog OC = 2 A) Maximum: 000 0110 0010 (bin) 98 (dec) (equivalent analog OC = 49 A) Note: Any values written to read-only registers are ignored.

OT_FAULT_LIMIT (4Fh)

Format	Literal (5-bit two's complement exponent, 11-bit two's complement mantissa)
Description	The OT_FAULT_LIMIT command sets the value of the temperature limit, in degrees Celsius, that causes an over-temperature fault condition when the sensed temperature from the external sensor exceeds this limit. Upon triggering the over-temperature fault, the following actions are taken: • Set the OTFW bit in the STATUS_BYTE register and STATUS_WORD register • Set the OTF and OTW bits in the STATUS_TEMPERATURE register • Notify the host (Asserts SMB_ALERT) • Generate internal signal/s CHx_TSD that eventually shut down the gate drivers. OT_FAULT_LIMIT is a paged register. In order to access this register for channel 1 of the device, PAGE must be set to 0. In order to access this register for channel 2 of the device , PAGE must be set to 1. For simultaneous access of channels 1 and 2, PAGE command must be set to 11. With regards to multi-phase operation: PAGE 0 can always be written to. PAGE 1 can be written only if it is a master (in effect, you can not write PAGE 1 if it is configured as a slave). In this case where PAGE 1 is a slave, the PAGE0 value is used for PAGE1/channel 2. Additionally, for 3-phase or 4-phase mode, the second IC PAGE 0 slave must be programmed by the user to have the same limit value as the master in IC 1 (in effect, the burden is on the user and can not be enforced by the hardware). An attempt to write a PAGE 1 SLAVE channel command results in a NACK'd command and the reporting of an IVC fault and triggering of SMB_ALERT. The OT_FAULT_LIMIT must always be greater than the OT_WARN_LIMIT. Writing a value to OT_FAULT_LIMIT less than or equal to OT_WARN_LIMIT causes the device to set the cml bit in the STATUS_BYTE register and the ivd bit in the STATUS_CML registers and assert SMB_ALERT.
Default	0000 0000 1010 0101 (binary) The default setting results in a real OT_FAULT_LIMIT of 165℃. The default power-up state can be changed using the STORE_USER commands.

r	r	r	r	r	r	r	r	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Exponent					Mantissa										

Bits	Field Name	Description
7:3	Exponent	(Format: two's complement) This is the exponent for the linear format. Default: 00000 (bin) 0 (dec) (represents mantissa with steps of 1℃) These default settings are not programmable. Note: Any values written to read-only registers are ignored.
2:0 7:0	Mantissa	(Format: two's complement) This is the Mantissa for the linear format. Default: 000 1010 0101 (bin) 165 (dec) (165℃) Minimum: 000 0111 1000 (bin) 120 (dec) (120℃) Maximum: 000 1010 0101 (bin) 165 (dec) (165℃) Note: Any values written to read-only registers are ignored.

Table. OT_FAULT THRESHOLD Settings

TEMPERATURE (℃)(1)	OT_FAULT_THRESHOLD (℃ BIN)	TEMPERATURE (℃)	OT_FAULT RESET THRESHOLD (℃ BIN)
120	01111000	100	01100100
125	01111101	105	01101001
130	10000010	110	01101110
135	10000111	115	01110011
140	10001100	120	01111000
145	10010001	125	01111101
150	10010110	130	10000010
155	10011011	135	10000111
160	10100000	140	10001100
165	10100101	145	10010001

(1) Lists only multiples of 5℃; but, the actual LSB is 1℃.

OT_WARN_LIMIT (51h)

Format	Literal (5-bit two's complement exponent, 11-bit two's complement mantissa)
Description	The OT_WARN_LIMIT command sets the value of the temperature, in degrees Celcius, which causes an over-temperature warning condition. • Sets the OTFW bit in the STATUS_BYTE register and STATUS_WORD register • Sets the OTW bit in the STATUS_TEMPERATURE register • Notifies the host (Asserts SMB_ALERT) OT_WARN_LIMIT is a paged register. In order to access this register for channel 1 of the device, PAGE must be set to 0. In order to access this register for channel 2 of the device, PAGE must be set to 1. For simultaneous access of channels 1 and 2, PAGE command must be set to 11. With regards to multi-phase operation: PAGE 0 can always be written to. PAGE 1 can be written only if it is a master (in effect, you can not write PAGE 1 if it is configured as a slave). In this case where PAGE 1 is a slave, the PAGE0 value is used for PAGE1/channel 2. Additionally, for 3-phase or 4-phase mode, the second IC PAGE 0 slave must be programmed by the user to have the same limit value as the master in IC 1 (in effect, the burden is on the user and can not be enforced by the hardware). An attempt to write a PAGE 1 SLAVE channel command results in a NACK'd command and the reporting of an IVC fault and triggering of SMB_ALERT. The OT_WARN_LIMIT should always be set to less than the OT_FAULT_LIMIT. Writing a value to OT_WARN_LIMIT greater than OT_FAULT_LIMIT causes the device to set the cml bit in the STATUS_BYTE register and the ivd bit in the STATUS_CML registers and assert SMB_ALERT.
Default	0000 0000 1000 1100 (binary) The default setting results in a real OT_WARN_LIMIT of 140℃. The default power-up state can be changed using the STORE_USER commands.

r	r	r	r	r	r	r	r	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Exponent					Mantissa										

Bits	Field Name	Description
7:3	Exponent	(Format: two's complement) This is the exponent for the linear format. Default: 00000 (bin) 0 (dec) (1℃) These default settings are not programmable. Note: Any values written to read-only registers are ignored.
2:0 7:0	Mantissa	(Format: two's complement) This is the Mantissa for the linear format. Default: 000 1000 1100 (bin) 140 (dec) (140℃) Minimum: 000 0110 0100 (bin) 100 (dec) (100℃) Maximum: 000 1000 1100 (bin) 140 (dec) (140℃) Note: Any values written to read-only registers are ignored.

Table. OT_WARN_LIMIT Settings

TEMPERATURE (℃)(1)	OT_FAULT_THRESHOLD (℃ BIN)	TEMPERATURE (℃)	OT_FAULT RESET THRESHOLD (℃ BIN)
100	01100100	80	1010000
105	01101001	85	1010101
110	01101110	90	1011010
115	01110011	95	1011111
120	01111000	100	1100100
125	01111101	105	1101001
130	10000010	110	1101110
135	10000111	115	1110011
140	10001100	120	1111000

(1) Lists only multiples of 5℃; but, the actual LSB is 1℃.

TON_RISE (61h)

Format	Linear
Description	The TON_RISE command sets the time in ms, from when the reference VREF starts to rise until it reaches the end value. It also determines the rate of transition of the reference VREF (either due to VREF_TRIM or STEP_VREF_MARGIN_HIGH/ STEP_VREF_MARGIN_LOW commands), when this transition is executed during the soft-start state. Values written within the supported range of TON_RISE are mapped to the nearest supported increment. TON_RISE is a paged register. In order to access this register for channel 1 of the device, PAGE must be set to 0. In order to access this register for channel 2 of the device, PAGE must be set to 1. For simultaneous access of channels 1 and 2, PAGE command must be set to 11. With regards to multi-phase operation: The user can always write to PAGE 0 (channel 1). PAGE 1 (channel 2) can be written only if it is a master (in effect, the user can not write PAGE 1 if it is configured as a slave). In this case where PAGE 1 is a slave, the PAGE0 value is used for PAGE1/channel 2. Additionally, for 3-phase or 4-phase mode, the second IC PAGE 0 slave must be programmed by the user to have the same limit value as the master in IC 1 (in effect, the burden is on the

	user and can not be enforced by the hardware). An attempt to write a PAGE 1 (channel 2) SLAVE channel command results in a NACK'd command and the reporting of an IVC fault and triggering of SMB_ALERT.
Default	The default setting results in TON_RISE of 2.7ms The default power-up state can be changed using the STORE_USER commands.

r	r	r	r	r	r	r	r	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Exponent					Mantissa										

Bits	Field Name	Description
7:3	Exponent	(Format: two's complement) This is the exponent for the linear format. Default: 11100 (bin) -4 (dec) (62.5 μs) These default settings are not programmable. Note: Any values written to read-only registers are ignored.
2:0 7:0	Mantissa	(Format: two's complement) This is the Mantissa for the linear format. Default: 000 0010 1011 (bin) 43 (dec) (equivalent to 2.688 ms) Minimum: Any value equal or less than 12 dec is equivalent to the min 600 μs Maximum: Any value greater than 120 dec is equivalent to 9 ms Note: Any values written to read-only registers are ignored.

Table . Allowable TON_RISE Values

TON_RISE TIME (ms)	MANTISSA (BINARY)
0.6	000 0000 1010
0.9	000 0000 1110
1.2	000 0001 0011
1.8	000 0001 1101
2.7	000 0010 1011
4.2	000 0100 0011
6	000 0110 0000
9	000 1001 0000

STATUS_BYTE (78h)

Format	Unsigned binary
Description	The STATUS_BYTE command returns one byte of information with a summary of the most critical faults. STATUS_BYTE is a paged register. In order to access this register for channel 1 of the device, PAGE must be set to 0. In order to access this register for channel 2 of the device, PAGE must be set to 1. For simultaneous access of channels 1 and 2, PAGE command must be set to 11. If configured as a master, each channel indicates faults on its own channel. However, if configured as a slave, the output voltage faults – OVF, UVF, PGOOD are only be set for that slave's master (which may be in the other IC for 3-ph and

	4-ph systems) while these faults for the slave are set to 0. Flags related to IOUT and TEMPERATURE (OCF, OCW, OTF, OTW) are set on PAGE 0 for channel 1 and PAGE 1 for channel 2, in all modes. The STATUS_BYTE register also reports communication faults in the Other Faults bit.
Default	0x000000 (binary)

7	6	5	4	3	2	1	0
0	OFF	OVF	OCF	VIN_UV	OTFW	cml	oth

Bits	Field Name	Description
7	0	Default: 0
6	OFF	(Format: binary) Output is OFF This bit is asserted if the unit is not providing power to the output, regardless of the reason, including simply not being enabled. 0: Unit is on 1: Unit is off
5	OVF	(= VOUT_OV in PMBus Specification) (Format: binary) Output Over-Voltage Fault Triggers SMB_ALERT. For a slave configuration, this bit is set to 0. 0: (Default) An output over-voltage fault has not occurred. 1: An output over-voltage fault has occurred.
4	OCF	(=IOUT_OC in PMBus Specification) (Format: binary) Output Over-Current Fault 0: (Default) An output over-current fault has not occurred. 1: An output over-current fault has occurred.
3	VIN_UV	(Format: binary) Input voltage (VIN) under-voltage fault. This bit is defined only on PAGE0. For PAGE1, this bit is 0. This bit is masked before soft-start is finished. 0: (Default) An input under-voltage fault has not occurred. 1: An input under-voltage fault has occurred.
2	OTFW	(= TEMPERATURE in PMBus Specification) (Format: binary) Over-Temperature Fault/warning OTF or OTW input has been asserted by the external sensor for that channel. 0: (Default) An over-temperature fault or warning has not occurred. 1: An over-temperature fault or warning has occurred.

1	cml	(= CML in PMBus Specification) (Format: binary) Communications, memory or logic fault has occurred. This bit is used to flag communications, memory or logic faults. 0: (Default) A communications, memory or logic fault has not occurred 1: A communications, memory or logic fault has occurred
0	oth	(= NONE OF THE ABOVE in the PMBus Specification) (Format: binary) Other Fault This bit is used to flag faults not covered with the other bit faults. In this case, UVF or OCW faults are examples of other faults not covered by the bits (7:1) in this register. 0: (Default) A fault or warning not listed in bits (7:1) has not occurred. 1: A fault or warning not listed in bits (7:1) has occurred.

STATUS_WORD (79h)

Format	Unsigned binary
Description	The STATUS_WORD command returns two bytes of information with a summary of the device's fault/warning conditions. STATUS_WORD is a paged register. In order to access this register for channel 1 of the device, PAGE must be set to 0. In order to access this register for channel 2 of the device, PAGE must be set to 1. If PAGE command is set to 11, then PAGE 0 of the status register is read. The STATUS_WORD also reports a power good fault. If configured as a master, each channel indicates faults on its own channel. However, if configured as a slave, the output voltage faults (OVF, UVF, PGOOD) are be set only for that slave's master (which may be in the other device for 3-phase and 4-phase systems) while these faults for the slave are set to 0. Flags related to IOUT and TEMPERATURE (OCF, OCW, OTF, OTW) are set on PAGE 0 for channel 1 and PAGE 1 for channel 2, in all modes. The STATUS_WORD also reports communication faults in the Other Faults bit.
Default	000000000x000000 (binary)

7	6	5	4	3	2	1	0	7	6	5	4	3	2	1
VF	OCFW	0	MFR	PGOOD_Z	0	0	0	0	OFF	OVF	OCF	VIN_UV	OTFW	cml

Bits	Field Name	Description
7	VF	(=VOUT in the PMBus Specification) (Format: binary) Voltage Fault = (OVF + UVF) For slave configurations, this bit is set to 0. 0: (Default) An output voltage fault or warning has not occurred. 1: An output voltage fault or warning has occurred.

6	OCFW	(= IOUT/POUT in the PMBus Specification) (Format: binary) Output Current Fault OR Warning = (OCF + OCW) 0: (Default) An output over-current fault or warning has not occurred. 1: An output over-current fault or warning has occurred.
5	0	Default: 0
4	MFR	(= MFR in the PMBus Specification) (Format: binary) Internal thermal fault (from bandgap) Thermal shutdown fault for the IC 0: (Default) An internal TSD has not occurred. 1: An internal TSD has occurred.
3	PGOOD_Z	(= POWER_GOOD# in the PMBus Specification) (Format: binary) Power Good Fault (in effect, Power Good Indication–Inverted) The Power Good fault is used to flag when the converter output voltage rises or falls outside of the PGOOD window. If the channel is configured as a slave, this bit are set to "0" (PGOOD_Z is only reflected in the master). 0: (Default) A Power Good fault is not present. 1: Device-channel experiencing a Power Good fault.
2:0	0	Default: 0

The STATUS_WORD low byte is the STATUS_BYTE.

STATUS_VOUT (7Ah)

Format	Unsigned binary
Description	The STATUS_VOUT command returns one byte of information relating to the status of the converter's output voltage related faults. The PMBus core is notified of these fault conditions via the 2 input pins labeled OVF and UVF. The PMBus core then communicates these faults to the host through its serial communication channel. STATUS_VOUT is a paged register. In order to access this register for channel 1 of the device, PAGE must be set to 0. In order to access this register for channel 2 of the device, PAGE must be set to 1. For simultaneous access of channels 1 and 2, PAGE command must be set to 11.
Default	00000000 (binary)

7	6	5	4	3	2	1	0
OVF	0	0	UVF	0	0	0	0

Bits	Field Name	Description
7	OVF	(= VOUT OV Fault in the PMBus Specification) (Format: binary)

		Output Over-Voltage Fault Set based upon the value stored in MFR_SPECIFIC_07 (D7h). If the channel is configured as a slave this bit are set to 0 (this bit is only reflected in the master). 0: (Default) An output over-voltage fault has not occurred. 1: An output over-voltage fault has occurred.
6:5	0	Default: 0
4	UVF	(= VOUT UV Fault in the PMBus Specification) (Format: binary) Output Under-Voltage Fault Set based upon the value stored in MFR_SPECIFIC_07 (D7h). If the channel is configured as a slave this bit are set to 0 (this bit is only reflected in the master). The UV fault indicates only an under-voltage condition at the FB pin and may not necessarily reflect an over-current situation. However, during an output crowbar short condition, the FB may sag below the UV threshold level before the current reaches the OC threshold, resulting in a UV fault. If the IOUT_OC_FAULT_RESPONSE register is selected to the retry setting, and the output short is persistent, an over-current fault are triggered for subsequent start-up retry attempts. 0: (Default) An output under-voltage fault has not occurred. 1: An output under-voltage fault has occurred.
3:0	0	Default: 0

STATUS_IOUT (7Bh)

Format	Unsigned binary
Description	The STATUS_IOUT command returns one byte of information relating to the status of the converter's output current related faults. The PMBus core is notified of these fault conditions via the inputs OCF and OCW. STATUS_IOUT is a paged register. In order to access this register for channel 1 of the device, PAGE must be set to 0. In order to access this register for channel 2 of the device, PAGE must be set to 1. For simultaneous access of channels 1 and 2, PAGE command must be set to 11.
Default	00000000 (binary)

7	6	5	4	3	2	1	0
OCF	0	OCW	0	0	0	0	0

Bits	Field Name	Description
7	OCF	(= IOUT OC Fault in the PMBus Specification) (Format: binary) Output Over-Current Fault Set based upon the value stored in IOUT_OC_FAULT_LIMIT 0: (Default) An output over-current fault has not occurred. 1: An output over-current fault has occurred.
6	0	Default: 0

5	OCW	(= IOUT OC Warning in the PMBus Specification) (Format: binary) Output Over-Current Warning Set based upon the value stored in IOUT_OC_WARN_LIMIT. 0: (Default) An output over-current warning has not occurred. 1: An output over-current warning has occurred.
4:0	0	Default: 0

STATUS_TEMPERATURE (7Dh)

Format	Unsigned binary
Description	The STATUS_ TEMPERATURE command returns one byte of information relating to the status of the converter's die temperature related faults. STATUS_TEMPERATURE is a paged register. In order to access this register for channel 1 of the device, PAGE must be set to 0. In order to access this register for channel 2 of the device, PAGE must be set to 1. For simultaneous access of channels 1 and 2, PAGE command must be set to 11.
Default	00000000 (binary)

7	6	5	4	3	2	1	0
OTF	OTW	0	0	0	0	0	0

Bits	Field Name	Description
7	OTF	(= OT Fault in the PMBus Specification) (Format: binary) Over-Temperature Fault 0: (Default) A temperature fault has not occurred. 1: A temperature fault has occurred.
6	OTW	(= OT Warning in the PMBus Specification) (Format: binary) Over-Temperature Warning 0: (Default) A temperature warning has not occurred. 1: A temperature warning has occurred.
5:0	0	Default: 0

STATUS_CML (7Eh)

Format	Unsigned binary
Description	The STATUS_ CML command returns one byte containing PMBus serial communication faults.
Default	00000000 (binary)

7	6	5	4	3	2	1	0
ivc	ivd	pec	mem	0	0	oth	0

Bits	Field Name	Description
7	ivc	(= Invalid/Unsupported Command in the PMBus Specification) (Format: binary) Invalid or unsupported Command Received 0: (Default) Invalid or unsupported Command not Received. 1: Invalid or unsupported Command Received. An attempt to write an invalid PAGE 1 SLAVE channel command results in a NACK'd command and the reporting of an IVC fault and triggering of SMB_ALERT.
6	ivd	(= Invalid/Unsupported Data in the PMBus Specification) (Format: binary) Invalid or unsupported data Received 0: (Default) Invalid or unsupported data not Received. 1: Invalid or unsupported data Received.
5	pec	(= Packet Error Check Failed in the PMBus Specification) (Format: binary) Packet Error Check Failed This is a CRC byte sent at the end of each data packet. It is implemented as CRC(x) = x8 + x2 + x1 + 1 0: (Default) Packet Error Check Passed 1: Packet Error Check Failed
4	mem	(= Memory Fault Detected in the PMBus Specification) (Format: binary) Memory Fault Detected This bit indicates a fault with the internal memory. 0: (Default) No fault detected 1: Fault detected
3:2	0	Default: 0
1	oth	(= Other Communication Fault in the PMBus Specification) (Format: binary) Other Communication Fault 0: (Default) A communication fault other than the ones listed in this table has not occurred. 1: A communication fault other than the ones listed in this table has occurred.
0	0	Default: 0

STATUS_MFR_SPECIFIC (80h)

Format	Unsigned binary
Description	The STATUS_ MFR_SPECIFIC command returns one byte containing manufacturer-specific faults or warnings.

Default	00000000 (binary)

7	6	5	4	3	2	1	0
otfi	x	x	ivaddr	ch1_sps_flt	ch2_sps_flt	ch1_slave	ch2_slave

Bits	Field Name	Description
7	otfi	(Format: binary) Over temperature fault internal. This bit is required to distinguish an over temperature fault internal to the device from an external temperature fault. 0: (Default) The internal temperature is below the fault threshold. 1: The internal temperature is above the fault threshold.
6:5	x	Default: 0
4	ivaddr	(Format: binary) Invalid PMBus address This bit is set when the PMBus address detection circuit does not resolve to a valid address. In this event, the device responds to the address: 127d. 0: (Default)
3	ch1_sps_flt	(Format: binary) Channel 1 smart power-stage fault This bit reports that the smart power-stage has declared a fault (either over-current or over-temperature) . 0: (Default)
2	ch2_sps_flt	(Format: binary) Channel 2 smart power-stage fault This bit reports that the smart power-stage has declared a fault (either over-current or over-temperature) . 0: (Default)
1	ch1_slave	(Format: binary) Channel 1 Slave This bit is set when channel 1 is configured as a slave channel (by pulling FB1 > 2.5 V before power-up). It is only used for internal read purposes and does not trigger SMBLERT. 0: (Default)
0	ch2_slave	(Format: binary) Channel 2 Slave This bit is set when channel 2 is configured as a slave channel (by pulling FB2 > 2.5 V before power-up). It is only used for internal read purposes and does not trigger SMBLERT. 0: (Default)

READ_VOUT (8Bh)

Format	Linear
Description	The READ_VOUT command returns two bytes of data in the linear data format that represent the output voltage. The exponent is set to –9 by VOUT_MODE. VOUT = Mantissa x $2^{Exponent}$ READ_VOUT is a paged register. In order to access READ_VOUT register for channel 1 of the device, PAGE(7),(0) must be set to 00. In order to access READ_VOUT register for channel 2 of the device, PAGE(7),(0) must be set to 01. PAGE register cannot be set to 11 for READ_VOUT command.
Default	0000h

r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Mantissa															

Bits	Field Name	Description
7：0	Mantissa	(Format: unsigned binary) This is the Mantissa for the linear format. Default: 0000 0000 0000 0000 (bin) 0 (dec) Note: Any values written to read-only registers are ignored.

READ_IOUT (8Ch)

Format	Linear
Description	The READ_IOUT command returns the output current in amps for each channel. The reading from the Measurement System must be manipulated in order to convert the measured value into the desired value (IOUT). Note: only positive currents are reported. Any computed negative current (For example, 0 measured current and –4 A IOUT_CAL_OFFSET) is reported as 0 A. READ_IOUT is a paged register. In order to access READ_IOUT register for channel 1 of the device, PAGE(7),(0) must be set to 00. In order to access READ_IOUT register for channel 2 of the device, PAGE(7),(0) must be set to 01. PAGE(7),(0) register cannot be set to 11 for READ_IOUT command.
Default	E0000h

r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Exponent					Mantissa										

Bits	Field Name	Description
7：3	Exponent	(Format: two's complement) This is the exponent for the linear format. Default: 11100 (bin) -4 (dec) (62.5 mA lsb) These default settings are not programmable. Note: Any values written to read-only registers are ignored.
2:0 7:0	Mantissa	(Format: two's complement) Default: 000 00000000 (bin) 0 (dec) Note: Any values written to read-only registers are ignored.

READ_TEMPERATURE_2 (8Eh)

Format	Linear
Description	The READ_TEMPERATURE_2 command returns the temperature in degrees Celsius of the current channel specified by the PAGE command.
Default	F064h

r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Exponent					Mantissa										

Bits	Field Name	Description
7:3	Exponent	(Format: two's complement) This is the exponent for the linear format. Default: 11110 (bin) –2 (dec) 0.25℃ These default settings are not programmable. Note: Any values written to read-only registers are ignored.
2:0 7:0	Mantissa	(Format: two's complement) Default: 000 0110 0100 (bin) 100 (dec) Note: Any values written to read-only registers are ignored.

PMBus_REVISION (98h)

Format	Linear
Description	The PMBus_REVISION command returns the revision of the PMBus to which the device is compliant. The device is compliant to revision 1.1 of the PMBus specification.
Default	00010001b

r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0

Bits	Field Name	Description
7:0	/	/

MFR_SPECIFIC_00 (D0h)

Format	Unsigned binary
Description	The MFR_SPECIFIC_00 register is dedicated as a user scratch pad
Default	0000h The default power-up state can be changed using the STORE_USER commands.

r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0

Bits	Field Name	Description
7:0		

MFR_SPECIFIC_04 (VREF_TRIM) (D4h)

Format	Linear
Description	The VREF_TRIM command is used to apply a fixed offset voltage to the reference voltage. VREF = 600 mV + (VREF_TRIM + STEP_VREF_MARGIN_x) x 2 mV The maximum trim range is 10% /–20% of nominal VREF (600 mV) in 2-mV steps. Permissible values are from 60 mV to–120 mV. Including settings from both VREF_TRIM and STEP_VREF_MARGIN_x commands, the net permissible range of VREF is 60 mV to–180 mV. If the commanded VREF_TRIM is outside its valid range, then that value is not accepted; it also causes the device to set the cml bit in the STATUS_BYTE register and the ivd bit in the STATUS_CML registers, and triggers SMB_ALERT. If the combined VREF set by VREF_TRIM and/or STEP_VREF_MARGIN_x is outside the acceptable range, it causes the device to set the cml bit in the STATUS_BYTE register and the ivd bit in the STATUS_CML registers, it triggers SMB_ALERT, and the VREF are set to the highest or lowest allowed value (based on the commanded level). The VREF transition occurs at the rate determined by the TON_RISE (61h) command if the transition is executed during soft-start. Any transition in VREF after soft-start occurs at the rate determined by the highest programmable TON_RISE of 9 ms. The VREF_TRIM has two data bytes formatted as two's complement binary integer and can have positive and negative values. If the channel is configured as a SLAVE, this command can not be accessed for that channel. Any writes to the SLAVE channel for this command is ignored. (In analog, the master programmed value are used in a multi-phase system. No special action needed from digital.) An attempt to write the SLAVE channel command, or when in AVS mode results in a NACK'd command and the reporting of an IVC fault and triggering of SMB_ALERT.
Default	0000h (Fixed Offset Voltage = 0 V) The default power-up state can be changed using the STORE_USER commands.

r/w^E	r*	r*	r*	r*	r*	r*	r*	r*	r*	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0

Bits	Field Name	Description
7:0	High Byte	(Format: binary) Default: 0000 0000 (bin) Minimum: 1111 1111 (bin) (sign extended) Maximum: 0000 0000 (bin) (sign extended) Bits 6:0 changes for sign extension but are not otherwise programmable
7:0	Low Byte	(Format: binary) Default: 0000 0000 (bin) 0 (dec) 0 mV Minimum: 1100 0100 (bin) –60 (dec) (–120 mV) (sign extended, twos compliment) Maximum: 0001 1110 (bin) 30 (dec) (60 mV) Bits 7:6 changes for sign extension but are not otherwise programmable

MFR_SPECIFIC_05 (STEP_VREF_MARGIN_HIGH) (D5h)

Format	Linear
Description	The STEP_VREF_MARGIN_HIGH command is used to increase the value of the reference voltage by shifting the reference higher. When the OPERATION command is set to Margin High, the reference increases by the voltage (in mV) indicated by this command. Thus, the changed reference is given by: VREF = 600 mV + (VREF_TRIM + STEP_VREF_MARGIN_HIGH) x 2 mV The maximum range is 0 to 10% (60 mV) of nominal VREF (600 mV) in 2mV steps. Including settings from both VREF_TRIM and STEP_VREF_MARGIN_x commands, the net permissible range of VREF is 60 mV to –180 mV. If the commanded STEP_VREF_MARGIN_HIGH is outside its valid range, then that value is not accepted; it also causes the device to set the cml bit in the STATUS_BYTE register and the ivd bit in the STATUS_CML registers, and triggers SMB_ALERT. If the combined VREF set by VREF_TRIM and/or STEP_VREF_MARGIN_x is outside the acceptable range, it causes the device to set the cml bit in the STATUS_BYTE register and the ivd bit in the STATUS_CML registers, it triggers SMB_ALERT, and the VREF are set to the highest or lowest allowed value (based on the commanded level). The VREF transition occurs at the rate determined by the TON_RISE (61h) command if the transition is executed during soft-start. Any transition in VREF after soft-start occurs at the rate determined by the highest programmable TON_RISE of 9 ms. This is a paged register. In order to access this register for channel 1 of the device, PAGE must be set to 0. In order to access this register for channel 2 of the device, PAGE must be set to 1. For simultaneous access of channels 1 and 2, PAGE command must be set to 11. If the channel is configured as a SLAVE, this command can not be accessed for that channel. Any writes to the SLAVE channel for this command are ignored. (In analog, the master programmed value is used in a multi-phase system. No special action needed from digital). An attempt to write the SLAVE channel command results in a NACK'd command and the reporting of an IVC fault and triggering of SMB_ALERT.
Default	0000 0000 0001 1110 (binary) The default power-up state can be changed using the STORE_USER commands.

r	r	r	r	r	r	r	r	r	r	r	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0

Bits	Field Name	Description
7:0	High Byte	(Format: binary) Default: 0000 0000 (bin) Minimum: 0000 0000 (bin) Maximum: 0000 0000 (bin) Note: Any values written to read-only registers are ignored.
7:0	Low Byte	(Format: binary) This specifies a positive offset voltage on to default VREF. Default: 0001 1110 (bin) 30 (dec) (60 mV = 10% percent) Minimum: 0000 0000 (bin) 0 (dec) (0 mV) Maximum: 0001 1110 (bin) 30 (dec) (60 mV = 10% percent)

MFR_SPECIFIC_06 (STEP_VREF_MARGIN_LOW) (D6h)

Format	Linear
Description	The STEP_VREF_MARGIN_LOW command is used to decrease the reference voltage by shifting the reference lower. When the OPERATION command is set to Margin Low, the output decreases by the voltage indicated by this command. Thus, the changed reference is given by: VREF = 600 mV + (VREF_TRIM + STEP_VOUT_MARGIN_LOW) x 2 mV .The maximum range is 0 to–20% (–120 mV) of nominal VREF (600 mV) in 2mV steps. Including settings from both VREF_TRIM and STEP_VREF_MARGIN_x commands, the net permissible range of VREF is 60 mV to–180 mV. If the commanded STEP_VREF_MARGIN_LOW is outside its valid range, then that value is not accepted; it also causes the device to set the cml bit in the STATUS_BYTE register and the ivd bit in the STATUS_CML registers, and triggers SMB_ALERT. If the combined VREF set by VREF_TRIM and/or STEP_VREF_MARGIN_x is outside the acceptable range, it causes the device to set the cml bit in the STATUS_BYTE register and the ivd bit in the STATUS_CML registers, it triggers SMB_ALERT, and the VREF is set to the highest or lowest allowed value (based on the commanded level). The VREF transition occurs at the rate determined by the TON_RISE (61h) command if the transition is executed during soft-start. Any transition in VREF after soft-start occurs at the rate determined by the highest programmable TON_RISE of 9 ms. This is a paged register. In order to access this register for channel 1 of the device, PAGE must be set to 0. In order to access this register for channel 2 of the device, PAGE must be set to 1. For simultaneous access of channels 1 and 2, PAGE command must be set to 11. If the channel is configured as a SLAVE, this command can not be accessed for that channel. Any writes to the SLAVE channel for this command are ignored. (In analog, the master programmed value is used in a multi-phase system. No special action needed from digital.) An attempt to write the SLAVE channel command results in a NACK'd command and the reporting of an IVC fault and triggering of SMB_ALERT.
Default	1111 1111 1110 0010 (binary) The default power-up state can be changed using the STORE_USER commands.

r/w^E	r*	r*	r*	r*	r*	r*	r*	r*	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0

Bits	Field Name	Description
7:0	High Byte	(Format: binary) Default: 1111 1111 (bin) (msb is sign bit) Minimum: 1111 1111 (bin) (sign extended) Maximum: 0000 0000 (bin) Bits 6:0 can change for sign extension but are not otherwise programmable
7:0	Low Byte	(Format: two's complement) This specifies a negative offset voltage on to default VREF. Default: 1110 0010 (bin) -30 (dec) (–60 mV = –10% percent) Minimum: 1100 0100 (bin) -60 (dec) (–120 mV = –20% percent) Maximum: 0000 0000 (bin) 0 (dec) (0 mV) Bits 7:6 can change for sign extension but are not otherwise programmable

MFR_SPECIFIC_07 (PCT_VOUT_FAULT_PG_LIMIT) (D7h)

Format	Unsigned binary integer
Description	The PCT_VOUT_FAULT_PG_LIMIT is to set the PGOOD, VOUT_UV and VOUT_OV limits. This is a paged register. In order to access this register for channel 1 of the device, PAGE must be set to 0. In order to access this register for channel 2 of the device, PAGE must be set to 1. For simultaneous access of channels 1 and 2, PAGE command must be set to 11. If the channel is configured as a SLAVE, this command can not be accessed for that channel. Any writes to the SLAVE channel for this command are ignored. (In analog, the master programmed value is used in a multi-phase system. No special action needed from digital.) An attempt to read and write the SLAVE channel command results in a NACK'd command and the reporting of an IVC fault and triggering of SMB_ALERT.
Default	XXXX XX10 (binary) The default power-up state can be changed using the STORE_USER commands.

r	r	r	r	r	r	r	r
7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	PG(1:0)

Bits	Field Name	Description
7:2	X	X indicates writes are ignored and reads are 0
1:0	PG(1:0)	(Format: binary) PG, UV, OV Limit Selection. Default: 10

Table lists the over-voltage, under-voltage, and power-good threshold voltages. Bit (13) of MFR_SPECIFIC_16 (E0h) register determines the overvoltage setting.

Table. OV, UV, PGOOD Threshold Values

PG(1)	PG(0)	UV_fault (%)	PG_low (%)	PG_high (%)	OV_fault (%)	OV_fault (mV)	OV SETTING
0	0	–16.8	–12.5	12.5	16.8	n/a	Tracking
0	1	–12.0	–7.0	7.0	12.0		
1	0	-29.0	–23.0	7.0	16.8		
1	1	–29.0	–23.0	7.0	12.0		
0	0	–16.8	–12.5	12.5	N/A	800	Fixed
0	1	–12.0	–7.0	7.0		700	
1	0	–29.0	–23.0	7.0		800	
1	1	–29.0	–23.0	7.0		700	

MFR_SPECIFIC_08 (SEQUENCE_TON_TOFF_DELAY) (D8h)

Format	Unsigned binary integer
Description	The SEQUENCE_TON_TOFF_DELAY command is used to set the delay for turning on the device and the delay for turning off the device as a ratio of TON_RISE. This is a paged register. In order to access this register for channel 1 of the device, PAGE must be set to 0. In order to access this register for channel 2 of the device, PAGE must be set to 1. For simultaneous access of channels 1 and 2, PAGE command must be set to 11. If the channel is configured as a SLAVE, this command can not be accessed for that channel. Any writes to the SLAVE channel for this command are ignored. In such a case, internally the TON_DELAY is set to the minimum value of 50 μs and TOFF_DELAY is set to zero (overriding any contents of EEPROM). An attempt to read and write the SLAVE channel command results in a NACK'd command and the reporting of an IVC fault and triggering of SMB_ALERT.
Default	000X 000X (binary) The default power-up state can be changed using the STORE_USER commands.

r/w^E	r/w^E	r/w^E	r	r/w^E	r/w^E	r/w^E	r
7	6	5	4	3	2	1	0
TON_DEL<2:0>			X	TOFF_DEL<2:0>			X

Bits	Field Name	Description
7:5	TON_DEL<2:0>	(Format: binary) Default: 000b TON_DELAY = TON_RISE x TON_DEL<2:0> This parameter controls the delay from when ON = 1 until soft-start sequence begins. The default value is 0 ms. (Start the VOUT ramp without delay)
4	X	X indicates writes are ignored and reads are 0
3:1	TOFF_DEL<2:0>	(Format: binary) Default: 000b TOFF_DELAY = TON_RISE x TOFF_DEL<2:0> This parameter controls the delay from when ON = 0 until the output is disabled. The default value is 0 ms. (Shut off the output without delay)
0	X	X indicates writes are ignored and reads are 0

Table . Delay Time Ratios

TON_DEL<2:0> TOFF_DEL<2:0>	DELAY TIME RATIO (MULTIPLE OF TON_RISE)
000	0
001	1
010	2

011	3
100	4
101	5
110	6
111	7

NOTE

If the device turns off due to a turn-off delay time, any attempt to turn on the device before the turn-off delay time expires should be avoided. The device is available to be turned on only after the turn-off delay time expires and the device has been turned off.

MFR_SPECIFIC_16 (COMM_EEPROM_SPARE) (E0h)

Format	Unsigned binary
Description	This register contains EEPROM backed bits brought out to the top of the digital block IO for possible future use by analog or digital circuits
Default	1011 0001 xxxx x011 (binary) The default power-up state can be changed using the STORE_USER commands.

COMM_EEPROM_SPARE							
r/w^E	r/w^E	r/w^E	r/w^E	r	r	r	r
15	14	13	12	11	10	9	8
PGOOD_DEL_EN	DIS_API_CNT	FIX_OVP_EN	DIS_SSPB				

COMM_EEPROM_SPARE							
r	r	r	r	r	r	r	r
7	6	5	4	3	2	1	0

Bits	Field Name	Description
15	PGOOD_DLY_EN	(format: binary, access: read/write) Default: 1b PGOOD Delay Enable This bit, when high, enable 2-ms delay for PGOOD detection during startup.
14	DIS_API_CNT	(format: binary, access: read/write) Default: 0b Disables 3-clock count for API valley active state This bit, when high, disables the 3-clock counter for API valley. When the bit is low, the counting is enabled whereby the API-valley function can remain active only 3 consecutive clock cycles before being inactive for another 3 clocks.

13	FIX_OVP_EN	(Format: binary, access: read/write) Default: 1b Enable fixed output voltage OV protection This bit, when high, enables fixed OV protection circuitry that is active after the BP3 and BP5 voltage comes up. When the bit is low, tracking OV protection is enabled instead and in this case, OV protection is enabled only after the soft-start sequence has completed.
12	DIS_SSPB	(Format: binary, access: read/write) Default: 1b Disable pre-bias initiation after soft-start sequence has completed. This bit affects the PWM signal only during prebias startup. When this bit is high, PWM switching begins only if the COMP voltage is higher than the PWM ramp valley. When this bit is low, PWM switching is forced to begin after soft-start sequence has completed, even when the COMP voltage is lower than PWM ramp valley.

MFR_SPECIFIC_21 (OPTIONS) (E5h)

Format	Unsigned binary
Description	This register is used for setting user selectable options for the controller.
Default	0111 1111 0000 0000 (binary) The default power-up state can be changed using the STORE_USER commands.

Common/Shared							
r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w
7	6	5	4	3	2	1	0
TCO	CH2_CSGAIN_SEL<2:0>		CH1_CSGAIN_SEL<1:0>		en_adc_cntl	EN_TSNS_FLT	EN_SPS

r	r	r	r	r	r	r/w^E	r/w
						SMB_OV	msps_flt

Bits	Field Name	Description
7	TCO	(Format: binary) Default: 0b Temperature compensation override 0: OCF, OCW thresholds and current measurements are temp compensated 1: Temperature compensation is "disabled" TCO is a non-paged bit. Any change on TCO bit is applied to both page 0 and page 1.
6:5	CH2_CSGAIN_SEL<1:0>	(Format: binary) 1:0> Default: 11b Ch2 current-share gain select This 2-bit bus is used to select the gain of the current-sharing circuit in channel 2. For high

		DCR/L ratios, the user can select lower gains for current-loop stability.
4:3	CH1_CSGAIN_SEL<1:0>	(Format: binary) Default: 11b Ch1 current-share gain select This 2-bit bus is used to select the gain of the current-sharing circuit in channel 1. For high DCR/L ratios, the user can select lower gains for current-loop stability. 00: 50 V/V gain 01: 40 V/V gain 10: 30 V/V gain 11: 20 V/V gain
2	en_adc_ctl	(Format: binary) Default: 1b Enable ADC Control Bit. 0: Disable ADC operation. 1: Enable ADC operation.
1	EN_TSNS_FLT	(Format: binary) Default: 1b Enable fault input from Smart power stage This bit, when high, makes the device sensitive to fault communication from the smart power stage. When this bit is low, the device ignores the fault indication from the smart power stage. Whether this bit is high or low, the device performs over temperature protection and declares OT fault when Smart power stage temperature is above the OT fault threshold.
0	EN_SPS	(Format: binary) Default: 1b（forbid change）
7:2		Note: Any values written to read-only registers are ignored.
1	SMB_OV	(Format: binary) Default: 0b Make SMBALERT an OV fault indicator. This has page 0 scope only (in effect, it is defined only on page 0; the page 1 bit is not used). 0: SMBALERT functions normally 1: SMBALERT reports only OV_FAULT
0	msps_flt	(Format: binary) Default: 0b (PAGE scope) 0: No effect upon SMBALERT 1: Masks SMBALERT assertion due to setting of STATUS_MFR_SPECIFIC(3) / STATUS_MFR_SPECIFIC(2) (corresponding to the CH1_SPS_FLT and CH2_SPS_FLT respectively).

MFR_SPECIFIC_22 (PWM_OSC_SELECT) (E6h)

Format	Unsigned binary
Description	This register is used for setting user selectable PWM phase configuration (sync enable, direction of frequency synchronization pulses - in or out - in a master channel and number of phases) in a multi-phase system.
Default	0000h The default power-up state can be changed using the STORE_USER commands.

r	r	r	r	r	r	r	r	r	r	r	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
											SYNC_MODE<1:0>		ENSYNC	PHASE	

Bits	Field Name	Description
7:0 7:5		Note: Any values written to read-only registers are ignored.
4:3	SYNC_MODE<1:0>	(Format: binary) Default: 00b Synchronization configuration for the oscillator These bits allow the user to configure the internal PWM oscillator clock in the PWM master channel 1 in one of several operating modes as described below. 1. To change this value, the user must change this value in the register, save it to the EEPROM and then reboot the device via power down for the new value to take effect. 2. If channel 1 is a slave, then these bits are internally forced to <1:1> indicating that external signals on the SYNC and PHDET pins must override the internal clock and phase zero signals. In a case of slave channel 1, any attempt to write a "0" to either one or both bits are treated as invalid data – in effect, the 'cml' bit in the STATUS_BYTE register and the 'ivd' bit in the STATUS_CML register are set, and SMB_ALERT asserted. 00: Self generated clock with internal phasing, switch positions 1 and 3 01: External clock on SYNC pin, but phasing is internal; switch positions 1 and 3 10: External clock on SYNC pin and external phase signal on PHDET pin; switch positions 1 and 3 11: External clock on SYNC pin and external phase signal on PHDET pin; switch positions 2 and 4 (forced for channel 1 slave)
2	ENSYNC	(Format: binary) Default: 0b Synchronization enable This bit, when high, enables the synchronization drivers. 0: Synchronization is disabled 1: Synchronization is enabled

1:0	PHASE	(Format: binary) Default: 00b Number of phases in the system (that involves the IC). This pair of bits is used to configure the number of phases in the power-supply system containing the IC. This information is then used inside the PWM oscillator to set the master switching frequency and channel phase angles. 1. To change this value, the user must change this value in the register, save it to the EEPROM and then reboot the device via power down for the new value to take effect. 2. If channel 1 is a slave, then the bit PHASE <1> is internally forced to 1 indicating that only 3-ph or 4-ph modes can be enabled. In such a case of slave channel 1, any attempt to write a "0" to this bit is treated as invalid data – in effect, the 'cml' bit in the STATUS_BYTE register and the 'ivd' bit in the STATUS_CML register are set, and SMB_ALERT asserted. 00: Independent, dual channel operation 01: Two-phase operation (within single IC) 10: Three-phase operation (between two ICs) 11: Four-phase operation (between two ICs)

NOTE

A 120° phase shift can be achieved between three phases at 3-phase plus 1-phase configuration, the 1-phase rail has the same phase as channel 1 of the master IC.

A 90° phase shift can be achieved between all four phases at all other configurations listed in the table. SYNC pins of two devices need to be connected, and PHSET pins of two devices need to be connected.

Table. Phase Configurations(1)

PHASE CONFIGURATIONS	MASTER IC			SLAVE IC		
	SYNC_MODE	ENSYNC	PHASE	SYNC_MODE	ENSYNC	PHASE
3-phase + 1-phase	00	1	10	11	1	10
4-phase	00	1	11	11	1	11
2-phase + 2-phase	00	(2)	11	11	(2)	11
2-phase + dual-output	00	(2)	11	11	(2)	11
Dual-output + dual-output	00	(2)	11	11	(2)	11

(1) For 3-phase plus 1-phase configuration and 4-phase configuration, SYNC_MODE, ENSYNC and PHASE can be programmed, saved to EEPROM at one time and then reboot the device for the new value to take effect.

(2) For all other configurations listed in the table, follow these steps to program two devices to avoid potential damage.

1. Set ENSYNC to 0 on each device.
2. Program SYNC_MODE and PHASE correctly at both devices, save to the EEPROM and then reboot the devices.
3. Set ENSYNC to 1 on each device to enable synchronization between two devices. No reboot is needed.

MFR_SPECIFIC_23 (MASK SMBALERT) (E7h)

Format	Unsigned binary
Description	The MFR_SPECIFIC_23 (MASK SMBALERT) command may be used to prevent a warning or fault condition from asserting the SMBALERT signal. This command is unique in that it is partially paged; and partially common/shared – since some faults are channel dependent; and others are channel independent. The upper 8 bits of this register always controls and accesses the shared/common set of faults, regardless of the (00h) PAGE setting. However, the control and access for the lower 8 bits of this register are (00h) PAGE dependent and controls or reflects the currently selected page. Only provides below two options for MASK_SMBALERT setting. ● When en_auto_ARA bit (auto Alert Response Address response) is enabled, all other bits in this PMBus register need to be disabled. ● When en_auto_ARA bit is disabled, any other bits in this PMBus register can be set as desired.
Default	0000h The default power-up state can be changed using the STORE_USER commands.

Common/Shared								PAGE0, PAGE1							
r/w	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w	r/w^E	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w^E
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
motfi	mprtcl_err	msmb_TO_err	mivc	mivd	mpec	mmem	en_auto_ARA	mOTF	mOTW	mOCF	mOCW	mOVF	mUVF	mPGOOD_Z	mVIN_UV

Bits	Field Name	Description
7	motfi	(Format: binary) Default: 0b 0: No effect upon SMBALERT 1: Masks SMBALERT assertion due to setting of STATUS_MFR_SPECIFIC(7)
6	mprtcl_err	(Format: binary) Default: 0b 0: No effect upon SMBALERT 1: Masks SMBALERT assertion due to setting of SMB Protocol Error from the PMBus interface module. One of 2 sources is STATUS_CML(1).
5	msmb_TO_err	(Format: binary) Default: 0b 0: No effect upon SMBALERT 1: Masks SMBALERT assertion due to setting of SMB_TIMEOUT from the PMBus interface module. One of 2 sources is STATUS_CML(1).
4	mivc	(Format: binary) Default: 0b 0: No effect upon SMBALERT 1: Masks SMBALERT assertion due to setting of STATUS_CML(7)
3	mivd	(Format: binary) Default: 0b

		0: No effect upon SMBALERT 1: Masks SMBALERT assertion due to setting of STATUS_CML(6)
2	mpec	(Format: binary) Default: 0b 0: No effect upon SMBALERT 1: Masks SMBALERT assertion due to setting of STATUS_CML(5)
1	mmem	(Format: binary) Default: 0b 0: No effect upon SMBALERT 1: Masks SMBALERT assertion due to setting of STATUS_CML(4)
0	en_auto_ARA	(Format: binary) Default: 0b Enables auto Alert Response Address response. When this feature is enabled, the hardware automatically masks any fault source currently set from re-asserting SMB_ALERT when this device responds to an ARA on the PMBus. This prevents PMBus "bus hogging" in the case of a persistent fault in a device that consistently wins ARA arbitration due to its device address. In contrast, when this bit is cleared, immediate re-assertion of SMB_ALERT is allowed in the event of a persistent fault and the responsibility is upon the host to mask each source individually. When WRITE_PROTECT is set to 20h, 40h or 80h, en_auto_ARA is enabled automatically.
7	mOTF	Functionality of mask bit: (Format: binary) Default: 0b 0: No effect upon SMBALERT 1: Masks SMBALERT assertion due to setting of STATUS_TEMPERATURE(7)
6	mOTW	Functionality of mask bit: (Format: binary) Default: 0b 0: No effect upon SMBALERT 1: Masks SMBALERT assertion due to setting of STATUS_TEMPERATURE(6)
5	mOCF	Functionality of mask bit: (Format: binary) Default: 0b 0: No effect upon SMBALERT 1: Masks SMBALERT assertion due to setting of STATUS_IOUT(7)
4	mOCW	Functionality of mask bit: (Format: binary) Default: 0b 0: No effect upon SMBALERT 1: Masks SMBALERT assertion due to setting of STATUS_IOUT(5)
3	mOVF	Functionality of mask bit: (Format: binary) Default: 0b

		0: No effect upon SMBALERT 1: Masks SMBALERT assertion due to setting of STATUS_VOUT(7)
2	mUVF	Functionality of mask bit: (Format: binary) Default: 0b 0: No effect upon SMBALERT 1: Masks SMBALERT assertion due to setting of STATUS_VOUT(4)
1	mPGOOD_Z	Functionality of mask bit: (Format: binary) Default: 0b 0: No effect upon SMBALERT 1: Masks SMBALERT assertion due to setting of STATUS_WORD(11)
0	mVIN_UV	Functionality of mask bit: (Format: binary) Default: 0b 0: No effect upon SMBALERT 1: Masks SMBALERT assertion due to setting of STATUS_BYTE(3)

MFR_SPECIFIC_30 (TEMP_OFFSET) (EFh)

Format	Unsigned binary
Description	This paged register is used for setting user selectable offset in the measured temperature. The specified offset value is added to the post-math digital output. The new, post-offset, post-averaging temperature is used for READ_TEMP_2 reporting and for temperature compensation of IOUT_CAL_GAIN for both reporting READ_IOUT, and OC_FAULT_LIMIT/WARN threshold setting.
Default	F800h The default power-up state can be changed using the STORE_USER commands.

r	r	r	r	r	r/W^E	r	r	r	r	r	r	r	r/W^E	r/W^E	r
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Exponent					Mantissa										

Bits	Field Name	Description
7:3	Exponent	(Format: two's complement) This is the exponent for the linear format. Default: 11111 (bin) –1 (dec) (LSB = 0.5 deg) These default settings are not programmable.
2:0 7:0	Mantissa	(Format: two's complement) Default: 000 (bin) 0 (dec) (0 deg) Minimum 7F8 = –8 x 0.5 deg = –4 deg Maximum 006 = 6 x 0.5 deg = 3 deg

MFR_SPECIFIC_44 (DEVICE_CODE) (FCh)

Format	Unsigned binary
Description	The DEVICE_CODE command returns a 12-bit unique identifier code for the device and a 4-bit device revision code.
Default	01E0h

r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0

Bits	Field Name	Description
7:0 7:4	Identifier Code	0000 0001 1110b : Device ID Code Identifier for the device
3:0	Revision Code	0000b : Revision Code (first silicon starts at 0)

Notes:

1. For additional information on Product Packaging please refer to www.mornsun-power.com. Packaging bag number: 58210321;
2. The maximum capacitive load offered were tested at nominal input voltage and full load;
3. Unless otherwise specified, parameters in this datasheet were measured under the conditions of Ta=25℃, humidity<75%RH with nominal input voltage and rated output load;
4. All index testing methods in this datasheet are based on our company corporate standards;
5. We can provide product customization service, please contact our technicians directly for specific information;
6. Products are related to laws and regulations: see "Features" ;
7. Our products shall be classified according to ISO14001 and related environmental laws and regulations, and shall be handled by qualified units.

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